Abstracted Microarchitecture: Example Core 2 (2008) and *Core i7 Sandybridge (2011)*

Throughput (tp) is measured in doubles/cycle. For example: 2 *(4)*
Latency (lat) is measured in cycles
1 double floating point (FP) = 8 bytes
Rectangles not to scale

Core 2 | *Core i7*

Memory hierarchy:
- Registers
- L1 cache
- L2 cache
- Main memory
- Hard disk

double FP:
scalar tp:
- 1 add/cycle
- 1 mult/cycle

vector (SSE) tp
- 1 vadd/cycle = 2 adds/cycle
- 1 vmult/cycle = 2 mults/cycle

fadd
fmul
ALU
load
store
execution units

ISA

internal registers

16 FP register

lat: 3 *(4)*
tp: 2 *(4)*

L1 Dcache

lat: 14 *(12)*
tp: 1 *(4)*

L2 cache
4 MB
16-way
64B CB

lat: 100
tp: 1/4

depends on platform

Main Memory (RAM)
4 GB

lat: millions
tp: ~1/250
(~1/100)

depends on platform

Hard disk
≥ 0.5 TB

out of order execution
superscalar

issue 6 µops/ cycle

RISC µops

CISC ops

instruction pool
(up to 96 *(168)* "in flight")

instruction decoder
(up to 5 ops/cycle)

L1 Icache

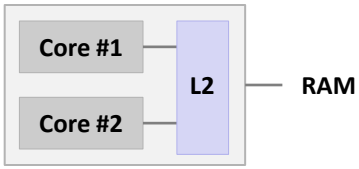
both:
32 KB
8-way
64B CB

CB = cache block

1 Core

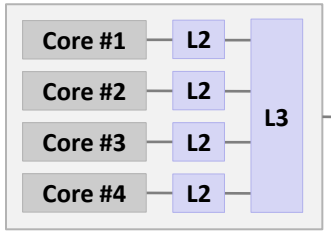
Core 2 Duo:

on die



Core i7 Sandy Bridge:
256 KB L2 cache
2–8MB L3 cache: lat 26-31, tp 4
RAM: tp 1
vector (AVX) tp
- 1 vadd/cycle = 4 adds/cycle
- 1 vmult/cycle = 4 mults/cycle

on die



Source: Intel manual (chapter 2)