PREDICTING WORST-CASE CHARGE BUILDUP IN POWER-DEVICE FIELD OXIDES†

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ABSTRACT

Existing models for worst-case charge buildup in silicon dioxide are applied to single- and two-level field plate termination structures in n-channel power MOSFETs. It is shown that the field-collapse model, when properly applied to these termination structures, provides excellent agreement between experimental and simulation worst-case breakdown-voltage degradation results. Nonuniform charge buildup in the termination structure field oxide is identified, and two methods of doing device simulation that take the nonuniformity into account are introduced. Finally, simple analytical models are presented that enable the nonuniform charge distribution to be calculated for any field-plate structure.

I. INTRODUCTION

In a vertical power DMOS (VDMOS) device, shown schematically in figure 1, the individual MOS cells are surrounded by the termination structure. The MOS Region defines the current handling capability of the device, while the Termination Region sets the breakdown voltage of the device [1]. Termination structures are built in the termination region to raise the breakdown voltage of the drain-body junction to near its ideal value. Field Plate (FP) termination structures are common in VDMOS devices, especially low-voltage, integrated devices, due to their small area consumption and relative processing ease [2]. FP structures, used in conjunction with highly-resistive Semi-Insulating Polycrystalline Silicon (SIPOS) films, are also found in high-voltage (1 *kV* or more) devices [3 – 6]. Finally, all integrated power devices have a "parasitic" FP in the form of the source contact [7]. Thus, the basic FP structure, and its response to ionizing radiation, is of great interest to power-device designers.

The field oxide (FOX) under the FP will collect charge in radiation environments, so the charge must be accounted for in the rad-hard power-device design process. Net positive oxide-trapped charge at the oxide-silicon interface, N_{ot}, degrades the breakdown voltage, BV, of n-channel power devices [8 – 10], and may degrade the breakdown voltage of p-channel power devices [11]. For power-device design purposes, only the worst-case value of N_{ot}, $N_{ot,wc}$, is of interest, since it is this value that must be considered when the voltage rating of the device is specified.

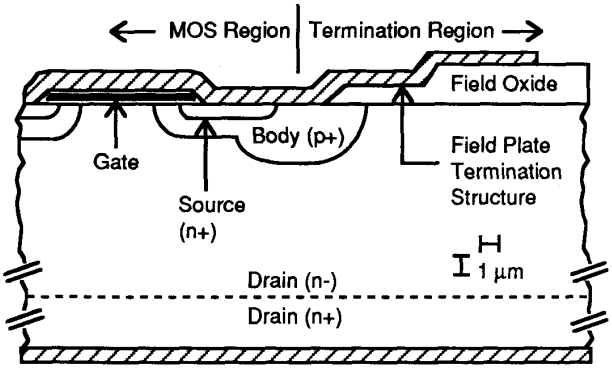

Figure 1. Representative cross section of an n-channel VDMOS power device.

This work introduces a technique for obtaining the $N_{ot,wc}$ distribution in a FP FOX, as well as methods to account for this distribution in device simulation. The methods are verified by comparing experimental breakdown-voltage degradation data with two-dimensional simulation results. Simple analytical equations are derived that enable prediction of the $N_{ot,wc}$ distribution in any FP FOX solely in terms of device parameters and applied voltage. The methods are simple and predictive, and can be used to gain insight into the charge buildup process in the FP FOX.

The device simulator used in this work was *A*rizona *S*emiconductor *P*ower Device *S*imulator (ASEPS) [8, 12]. ASEPS solves Poisson's equation in two dimensions and determines breakdown voltage by computing the ionization integral. ASEPS' numerical algorithms are specifically tailored for solving highly reverse-biased junctions; its rapid execution speed, guaranteed convergence, and flexible input format make it a powerful tool for power-device simulation and design.

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II. Experiment

A. Method

To predict worst-case charge buildup in the FP FOX, the radiation response of the FOX under the bias polarity present during normal operation of the power device must be determined. Lateral p-channel transistors with FOX as the gate dielectric, shown in figure 2a, were used for this purpose. Relevant device parameters of the n-channel power DMOS transistors with FP are shown in figure 2b. Only the termination region is shown, since it alone determines the BV of the device. The pre-irradiation BV of all the DMOS devices was approximately 200 V.

The FOX in both devices in figure 2 comes from the same process; the thickness difference between the two device types was a result of longer growth time for the FOX in figure 2a. Note that the thickness difference is not crucial, since the role of the device in figure 2a is only to identify the appropriate model for worst-case charge buildup in the FOX.

Several samples of both devices were concurrently irradiated in a Co-60 source (dose rate approximately 20 *rad(Si)/min*). During irradiation, both device types were biased at a constant voltage, V_{tot}, of either 0 V or 100 V. Charge buildup in the FOX transistors and breakdown voltage of the DMOS devices was measured at several values of total ionizing dose, D. Charge buildup was measured in the p-channel FOX devices using the mid-gap method [13], and BV of the DMOS devices was defined as V_{DS} when I_{DS} = 1 mA.

B. Results

The experimental N_a and breakdown voltage degradation, ΔBV, vs. D curves are shown in figure 3a and 3b, respectively. Negligible N_{it} formation was observed in the p-channel FOX devices, indicating negligible N_{it} formation in the FP FOX as well.

As shown in figure 3a, saturation of N_a buildup in the device of figure 2a is bounded by the prediction of the field-collapse (FC) model for negatively-biased oxides [14]. The FC model asserts that N_{ot} buildup saturates when the trapped charge in the oxide compensates the charge on the gate electrode. The electric field in the oxide goes to zero, and subsequent electron-hole pairs, *ehps*, efficiently recombine, leading to negligible additional charge buildup. Under this assumption, $N_{ot,wc}$ is [14]

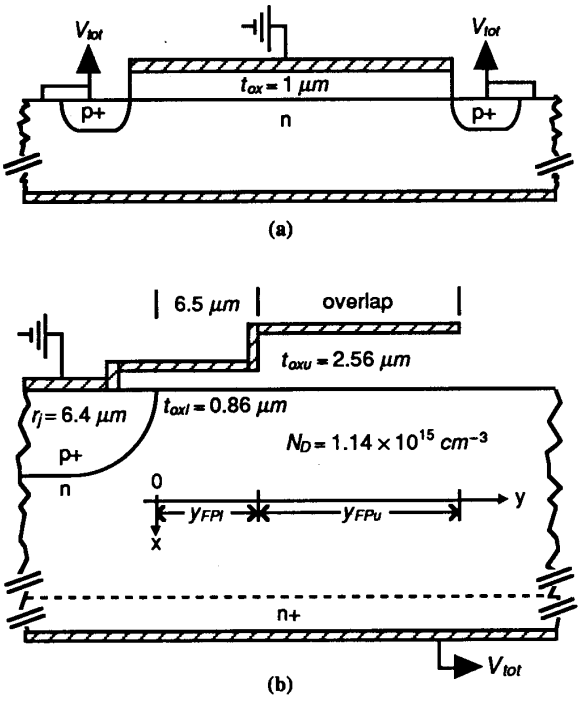

Figure 2. Schematic cross-sections of devices described in text. (a) P-channel lateral FOX transistor. (b) Termination region of n-channel DMOS transistors with FP termination structures.

$$N_{ot,wc} = \frac{C_{ox}|V_{ox}|}{q} \qquad (1)$$

where V_{ox} is the voltage across the oxide, C_{ox} is the oxide capacitance per unit area, and q is the magnitude of the electronic charge. In the device of figure 2a, the negatively-biased gate forms an inversion layer in the silicon, so most of the applied voltage is dropped across the FOX. That is, $V_{ox} \approx V_{tot}$, and equation (1) gives $N_{ot,wc} = 2.16 \times 10^{12}$ cm^{-2}, which is indicated at the top of figure 3a. Note also that when $V_{tot} = 0$ V, equation (1) predicts that $N_{ot,wc} = 0$ cm^{-2}, which, although clearly an approximation, is consistent with the bottom curve of figure 3a. In fact, the metal-silicon work-function difference, if taken to be on the order of a 1 V, gives $N_{ot,wc} = 2.15 \times 10^{10}$ cm^{-2}, which is a more realistic value. Thus, the FC model, as expressed in equation (1), adequately predicts $N_{ot,wc}$ for the device of figure 2a.

As indicated in figure 3b, ΔBV, and thus N_a buildup under the FP, saturates for D > 75 *krad(Si)* for the DMOS devices biased at $V_{tot} = -100$ V. The devices with $V_{tot} = 0$ V had

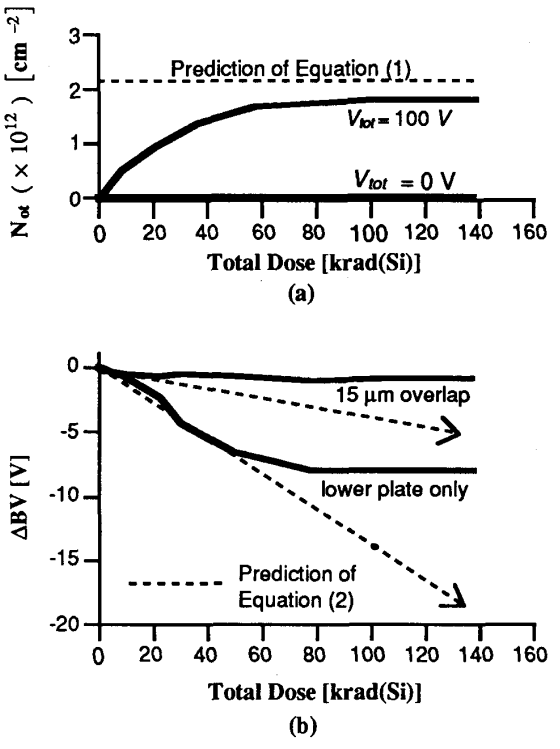

Figure 3. Comparison of experimental data (heavy lines) and predicted response (dashed lines). (a) N_{ot} vs. D for device of figure 2a. (b) ΔBV vs. D for devices of figure 2b.

ΔBV = 0 V for all values of D; this data is not shown in figure 3b or in subsequent figures. The ΔBV vs. D results are qualitatively consistent with the predictions of the FC model. Applying the FC model as expressed in equation (1) directly to the DMOS device is not appropriate, however, since it would greatly overestimate the maximum breakdown-voltage degradation of the structure, $\Delta BV(max)$. This issue, along with a brief review of previous work in modeling charge buildup in power-device termination structures, is addressed in the next section.

III. Charge Buildup In The DMOS FOX

A. Previous Work

Earlier modeling of breakdown voltage degradation of power MOSFETs [8, 10] has assumed that N_{ot} in the termination structure FOX increases linearly with D via

$$N_{ot} = D\, t_{ox}\, G\, F\,, \qquad (2)$$

where G is the generation rate of *ehps* per unit volume and F is the equivalent fraction of holes trapped at the oxide-silicon interface. For worst-case calculations at low total doses, it has been assumed that F = 1.0 [15]. In later work [8, 10], F has been determined by fitting equation (2) to experimental data.

It is seen immediately that equation (2) is of limited utility for estimating worst-case N_{ot} buildup in the FP FOX. That is, although an appropriate value for F can be found for the devices biased at V_{tot} = 0 V, (F = 0), an appropriate value for F cannot be found for the biased devices because, as mentioned previously, ΔBV, and thus N_{ot} buildup, saturates for $D > 75$ *krad(Si)*. Equation (2) can only be applied if it is recognized that F is a function of electric field in the oxide, which, in turn, is a function of N_{ot} already in the oxide. This analysis must be performed iteratively by computer. The result of such an analysis for the bias condition depicted in figure 2 is essentially equation (1) [14].

The assumption implicit in equation (2) is that N_{ot} buildup is uniform across the entire structure. This is a gross approximation, as will be shown in the next section.

B. Application of the Field-Collapse Model to the FP FOX

Since the FC model adequately predicted $N_{ot,wc}$ for the devices of figure 2a, it seems likely that the FC model, when properly applied, can predict $N_{ot,wc}$ in the FP FOX, and thus predict $\Delta BV(max)$ for the devices of figure 2b. If equation (1) is blindly used for this purpose (that is, let t_{ox} = 0.86 μm and $V_{ox} = V_{tot}$ in equation (1)), $N_{ot,wc}$ = 2.5 × 10^{12} cm^{-2}. If this value of N_{ot} is then used in an ASEPS simulation of the device of figure 2b, ΔBV is very large for all devices, regardless of overlap (greater than 30 V). However, experimental $\Delta BV(max)$ of the DMOS device with lower plate only was 8 V, and $\Delta BV(max)$ of the device with 15 μm overlap was 1.5 V. Devices with 5 and 10 μm overlaps had experimental $\Delta BV(max)$ of 6 and 4 V, respectively. Clearly, naive application of equation (1) overestimates $N_{ot,wc}$ in the DMOS FOX.

The reason equation (2) can be used directly to predict $N_{ot,wc}$ for the structure of figure 2a is that $V_{ox} \approx V_{tot}$. However, $V_{ox} < V_{tot}$ in an FP structure due to the large voltage drop in the depletion layer under the FP, which is supported by the adjacent p^+-n junction. Furthermore, V_{ox} varies with lateral position, y. These facts explain why naive application of the FC model to the FP FOX was unsuccessful. A more sophisticated application of the FC model is needed. This requires that the operation of the FP termination structure be

examined to uncover the physical mechanisms that lead to breakdown-voltage degradation in ionizing-radiation environments.

The means by which the FP raises the BV of the device, and the reason N_{α} degrades BV, can be interpreted with charge-balancing arguments. Note that under normal n-channel DMOS bias conditions, the x-component of the electric field in the FOX is negative. Electric field lines originate on positive ionized donors in the depletion layer under the FP and terminate on either negative charge on the FP or on ionized acceptors in the p^+ body. It is the termination of depletion-layer charge on the FP that gives rise to the finite E_x in the oxide; the finite E_x also raises the BV of the junction.

Under these bias conditions, ionizing-radiation-induced holes will drift toward the FP and possibly be trapped near the oxide-metal interface, where they compensate negative charge on the FP. As more positive charge accumulates, fewer positive ions will be uncovered in the depletion layer, and as a result the BV of the device degrades.

The FC model holds that charge buildup will continue in the DMOS FOX until E_x goes to zero at every point in the oxide. This can only happen when the trapped hole distribution in the oxide compensates charge on the FP such that the "effective" voltage on the FP seen from the semiconductor is the same as the surface potential of the *unterminated* junction. That is, the trapped holes must entirely negate any effect of the FP, as seen from the semiconductor, in order to force E_x to zero at every position y in the FOX. In terms of measurable quantities, the trapped hole distribution forces the pre-irradiation surface potential under the FP, $\psi_{s,FP}(y)$ to be the same as the surface potential of the unterminated p^+-n junction, $\psi_{s,pn}(y)$. The charge required to bring about this shift in $\psi_s(y)$ is seen to be directly proportional to the change in $\psi_s(y)$. $N_{ot,wc}(y)$ can be obtained, then, by finding $\psi_{s,FP}(y)$, subracting it from $\psi_{s,pn}(y)$, and using this difference in equation (1). Explictly,

$$N_{ot,wc}(y) = \frac{C_{ox}\left(\psi_{s,pn}(y) - \psi_{s,FP}(y)\right)}{q} \qquad (3)$$

can be used to approximate $N_{ot,wc}(y)$ in the FP FOX. The only approximation in equation (3) is using C_{ox}; the appropriate capacitance for the voltage difference is actually the series combination of C_{ox} and depletion-layer capacitance, C_{dep}. Since this combination, if it were taken into account, would only underestimate $N_{ot,wc}(y)$, the approximation does not affect the worst-case nature of the method.

C. Results

The structure with 15 μm overlap will be used to illustrate the methods outlined in the previous section. To demonstrate the generality of the methods, they will also be applied to the structure with lower plate only. In the graphs that follow, data points are simulation results, while dashed lines are analytical model predictions. The model is covered in the Appendix.

Figure 4 shows $\psi_{s,FP}(y)$ and $\psi_{s,pn}(y)$ of the structure with 15 μm overlap. A schematic of the two-level FP structure is provided for reference. Figure 5 shows $N_{ot,wc}(y)$ as defined by equation (3), using $\psi_{s,FP}(y)$ and $\psi_{s,pn}(y)$ from figure 4.

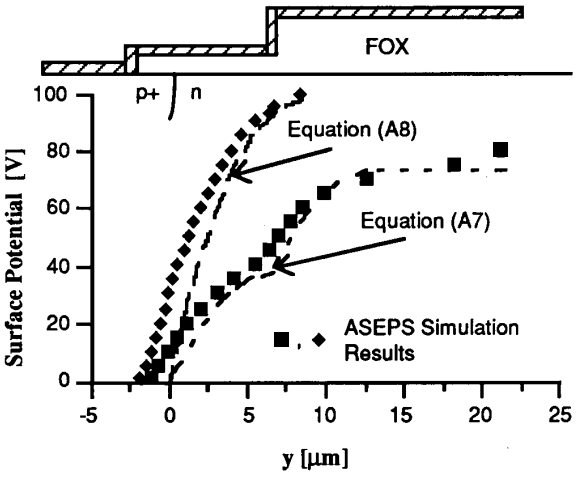

Figure 4. Surface potential under the two-level FP and of the unterminated junction.

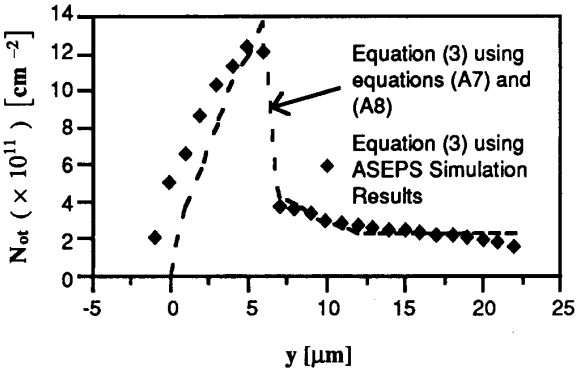

Figure 5. $N_{ot,wc}$ under the two-level FP.

The $N_{ot,wc}(y)$ profile under the two-level FP is highly nonuniform, and attains its maximum value, $N_{ot,wc}(max)$ near the edge of the lower FP. $N_{ot,wc}(max)$ is approximately

1.3×10^{12} cm^{-2}, which is far less than the 2.5×10^{12} cm^{-2} predicted by naive application of the FC model.

D. *Accounting for Nonuniform* N_{ot} *in Device Simulation*

All currently-available device simulators do not handle nonuniform N_a distributions. However, the effect of the $N_{ot,wc}(y)$ profile on $\psi_s(y)$, and thus on $\Delta BV(max)$, can be reproduced without this capability.

One way to account for the $N_{ot,wc}(y)$ distribution is to find its average value under the FP, $\overline{N_{ot,wc}}$, given by

$$\overline{N_{ot,wc}} = \frac{1}{y_{FPl} + y_{FPu}} \int_0^{y_{FPl} + y_{FPu}} N_{ot,wc}(y)\, dy \quad (4)$$

and perform the simulation with uniformly-distributed N_a equal to $\overline{N_{ot,wc}}$. Using the $N_{ot,wc}(y)$ data in figure 5, $\overline{N_{ot,wc}} = 5.1 \times 10^{11}$ cm^{-2}. ASEPS simulations with uniformly-distributed N_{ot} equal to $\overline{N_{ot,wc}}$ gives $\Delta BV(max) = 4$ V.

If still more accurate simulation results are desired, the $N_{ot,wc}(y)$ distribution in figure 5 must be taken into account explicitly. That is, instead of modeling the trapped holes by N_a at the oxide-silicon interface, the same effect can be achieved by altering the potential on the FP to reflect the presence of the trapped holes at the oxide-metal interface. This is done by segmenting the FP into many segments, and assigning each segment a different bias, $V_{FP,i}$, given by

$$V_{FP,i} = \overline{\psi_{s,pn}(y)}_i - \overline{\psi_{s,FP}(y)}_i . \quad (5)$$

In equation (5), i = 1...*# of segments* and $\overline{\psi_{s,pn}(y)}_i$ and $\overline{\psi_{s,FP}(y)}_i$ denote the average value of $\psi_{s,pn}(y)$ and $\psi_{s,FP}(y)$ through the ith segment. The concept is illustrated schematically in figure 6.

ASEPS simulations with segmented FP biased at $V_{FP,i}$ give $\Delta BV = 3$ V. ASEPS simulation output, both before irradiation and with segmented FP, is shown in figure 7. The lines are equipotential lines and circles indicate highest-field points.

Figure 8 presents ASEPS estimates of $\Delta BV(max)$ for the structure with 15 μm overlap obtained three different ways. Line (A) was obtained by segmenting the FP and biasing each segment separately, as shown schematically in figure 6; line (B) was obtained by assuming uniformly-distibuted N_a equal to $\overline{N_{ot,wc}}$; and line (C) was obtained by assuming uniformly-distributed N_a equal to $N_{ot,wc}(max)$. Clearly, agreement between simulation and experiment is improved by accounting for the $N_{ot,wc}(y)$ distribution when doing device simulations. Figure 9 presents the same information as figure 8 for the structure with lower plate only, illustrating the generality of the methods outlined above.

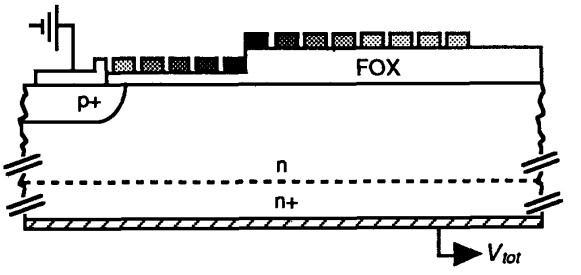

Figure 6. Schematic illustration of segmented FP for device simulation. Darker segments have larger V_{FP} applied to them.

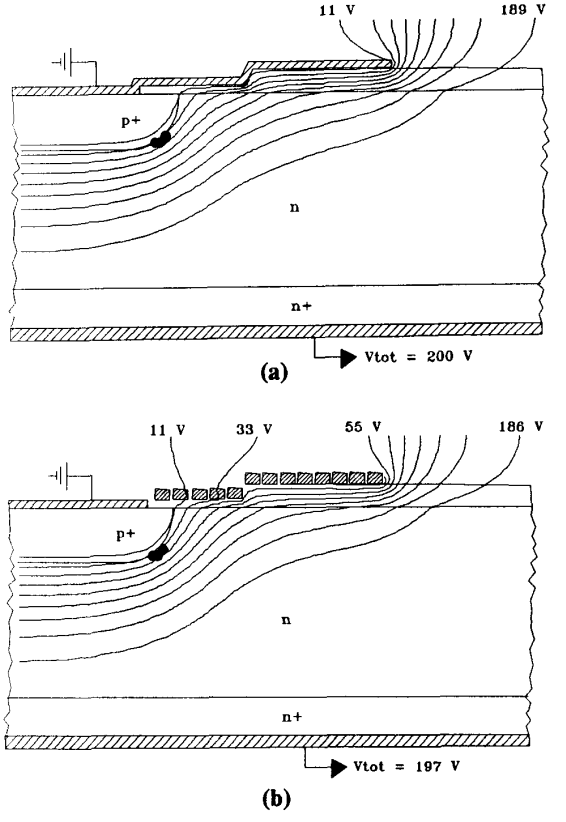

Figure 7. ASEPS simulation output. (a) Two-level FP with BV = 200 V, $N_a = 0$ cm^{-2}. (b) Segmented two-level FP as in figure 6. $BV = 197$ V.

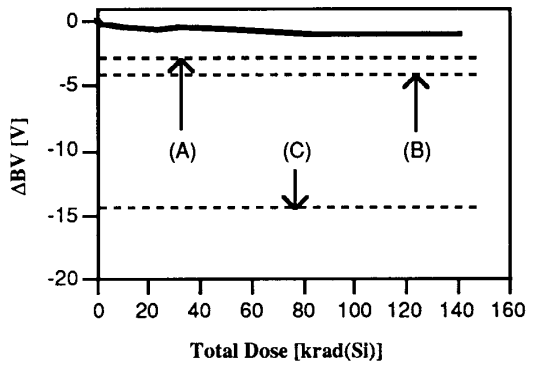

Figure 8. ΔBV vs. D for the DMOS device with 15 μm overlap. The heavy line is experimental data. (A), (B), and (C) represent ASEPS estimates of $\Delta BV(max)$, as described in the text.

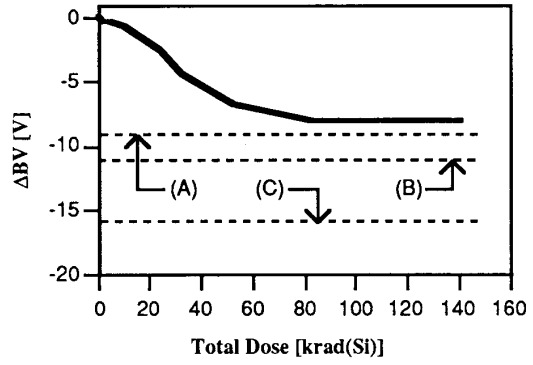

Figure 9. ΔBV vs. D for the device with lower plate only. The heavy line is experimental data. (A), (B), and (C) represent ASEPS estimates of $\Delta BV(max)$, as described in the text.

It is seen that by accounting for the nonuniform charge buildup, simulation results of $\Delta BV(max)$ closely approximate experimental data. The segmented FP gives more accurate estimates of $\Delta BV(max)$ than does equation (3), but it is also somewhat more cumbersome. Note, however, that the segmented FP method employs no approximations whatsoever, beyond discretizing the continuous $\psi_{s,pn}(y)$ and $\psi_{s,FP}(y)$ distributions. If nonuniform N_a were somehow incorporated into the simulation, the $N_{ot,wc}(y)$ distribution would necessarily be approximate due to the uncertainties in the correct value of capacitance at every point under the FP, as discussed at the end of section III.B.

The utility of precise knowledge of the $N_{ot,wc}(y)$ distribution in the DMOS FOX for device simulation has been established. Simple equations for determining $\psi_{s,FP}(y)$ and $\psi_{s,pn}(y)$, which can be used directly in equation (4) to obtain $N_{ot,wc}(y)$, are presented in the Appendix.

IV. Summary

Existing models for charge buildup in silicon dioxide were applied to power-device field oxides with the purpose of estimating worst-case charge buildup. Proper application of the field-collapse model allowed an estimate of the $N_{ot,wc}(y)$ distribution in the FP FOX to be generated. Two methods of taking this distribution into account for device simulation were introduced. Agreement between experimental and simulation $\Delta BV(max)$ was excellent, validating the method of obtaining $N_{ot,wc}(y)$. Simple equations are presented that allow the $N_{ot,wc}(y)$ distribution to be generated for any FP structure in terms of device parameters and applied voltage.

Appendix

The first step in obtaining $\psi_{s,FP}(y)$ is to find the maximum voltage across the oxide, $V_{ox}(max)$. $V_{ox}(max)$ is entirely determined by the characteristics of the depleted MOS capacitor that exists under the FP far from the drain-body junction. $V_{ox}(max)$ can be found in closed form by solving for the maximum value of the surface potential, $\psi_{s,FP}(max)$, and noting that $V_{ox}(max) = V_{tot} - \psi_{s,FP}(max)$.

Far from both the drain-body junction and the edge of the FP, and with negligible N_{ot} in the FOX, Gauss' law at the oxide-silicon interface is

$$\kappa_{ox} E_{ox} = \kappa_{Si} E_{Si}, \tag{A1}$$

where E_{ox} and E_{Si} are the x-components of the electric field in the oxide and silicon, and κ_{ox} and κ_{Si} are the relative permittivities of silicon dioxide and silicon, respectively. Using the depletion approximation in the x-direction, $\psi_{s,FP}(max)$ can be written as

$$\psi_{s,FP}(max) = \frac{\kappa_{Si}\,\varepsilon_o E_{Si}(max)^2}{2\,q\,N_D}, \tag{A2}$$

where $E_{Si}(max)$ is the maximum value of E_{Si}, N_D is the doping of epitaxial drain, and ε_o is the permittivity of free space. Solving equation (A1) for E_{Si}, and noting that $E_{ox}(max) = V_{ox}(max)/t_{ox}$, it follows that $E_{Si}(max)$ is

$$E_{Si}(max) = \frac{\kappa_{ox}\left(\psi_{s,FP}(max) - V_{tot}\right)}{\kappa_{Si}\, t_{ox}}. \qquad \text{(A3)}$$

Substituting equation (A3) into equation (A2) and solving the resulting quadratic equation for $\psi_{s,FP}(max)$ gives

$$V_{ox}(max) = \frac{\gamma}{2}\left[\sqrt{4\,V_{tot} + \gamma^2} - \gamma\right], \quad \text{where } \gamma \equiv \frac{\sqrt{2\,q\,N_D\,\kappa_{Si}\,\varepsilon_o}}{C_{ox}} \qquad \text{(A4)}$$

Note that both the upper and lower FP have a characteristic $V_{ox}(max)$. Accordingly, lower-plate quantities will be denoted by a subscript l and upper-plate quantities by a subscript u.

The $\psi_{s,FP}(y)$ relationship can be approximated by standard one-dimensional abrupt junction equations. Therefore, the distance from the metallurgical junction, y_{critl}, where $V_{oxl}(max)$ is first reached is written

$$y_{critl} = \sqrt{\frac{2\,\kappa_{Si}\,\varepsilon_o\,V_{oxl}\,(max)}{q\,N_D}}, \qquad \text{(A5)}$$

and the distance from the lower FP where $V_{oxu}(max)$ is first reached, y_{critu}, is

$$y_{critu} = \sqrt{\frac{2\,\kappa_{Si}\,\varepsilon_o\left(V_{oxu}\,(max) - V_{oxl}\,(max)\right)}{q\,N_D}} \qquad \text{(A6)}$$

The complete $\psi_{s,FP}(y)$ relationship is given by equation (A7). Equation (A7) is compared to simulation results in figure 4. The agreement is quite good, although it could be improved by including the finite drop in the diffused p^+ region and the field crowding effects near the ends of the FP.

The $\psi_{s,pn}(y)$ relationship can be approximated by the $V(r)$ relationship, where r is the radius vector in cylincrical coordinates, for a cylindrical one-sided p^+-n junction. $V(r)$ is given by [1]

$$V(r) = \frac{q\,N_D}{2\,\kappa_{Si}\,\varepsilon_o}\left[\frac{r_j^2 - r^2}{2} + r_d^2\,ln\left(\frac{r}{r_j}\right)\right] \text{ for } r_j \le r \le r_d, \qquad \text{(A8)}$$

where r_j is the junction radius and r_d is the depletion-layer radius, which is found by letting $V(r) = V_{tot}$ and iterating on r until equation (A8) is satisfied. The relationship between y and r is illustrated in figure A1. Note that the variable substitutions $r' = r - r_j$, $r_d' = r_d - r_j$ were used in equation (A8) for comparison to ASEPS simulation data or equation (A7), and that the direction of r was taken to be in the direction of y. Note also that cylindrical geometry implicitly assumes the aspect ratio for lateral diffusion is 1.0 instead of 0.8 - 0.85, as it is in physical diffused p^+-n junctions, and was in the ASEPS simulations.

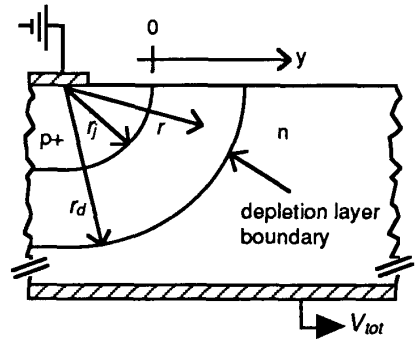

Figure A1. Coordinate conventions for cylindrical abrupt p^+-n junction.

The agreement between simulation and equations (A7) and (A8) is quite good despite the approximations made in the development of the equations. Clearly, the equations are suitable for first-order design and analysis purposes, and can be used to obtain an estimate of $N_{ot,wc}(y)$ under the FP without doing any two-dimensional simulations of the structure.

$$\psi_{s,FP} = \begin{cases} 0 & (y \le 0) \\ \frac{-qN_D}{2\,\kappa_{Si}\,\varepsilon_o}(y_{critl} - y)^2 + V_{oxl}(max) & (0 \le y \le y_{critl}) \\ V_{oxl}(max) & (y_{critl} \le y \le y_{FPl}) \\ \frac{-qN_D}{2\,\kappa_{Si}\,\varepsilon_o}(y_{critu} + y_{FPl} - y)^2 + V_{oxu}(max) & (y_{FPl} \le y \le y_{critu} + y_{FPl}) \\ V_{oxu}(max) & (y_{critu} + y_{FPl} \le y \le y_{FPu} + y_{FPl}) \end{cases} \qquad \text{(A7)}$$

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