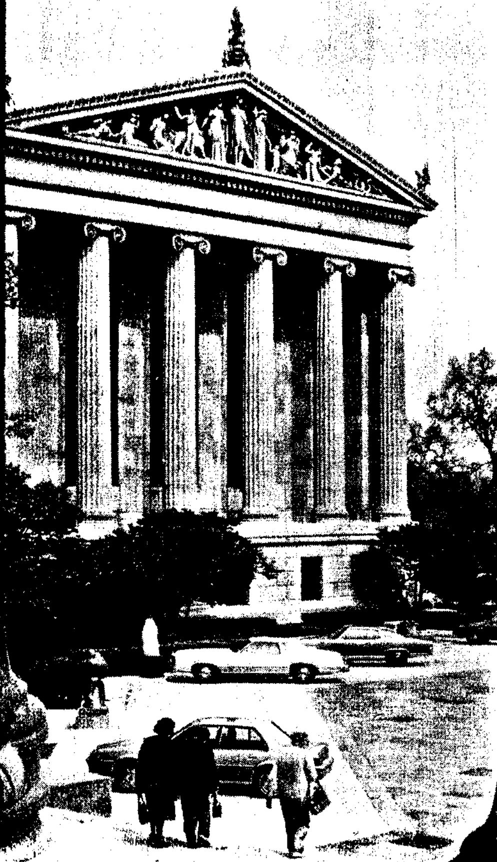
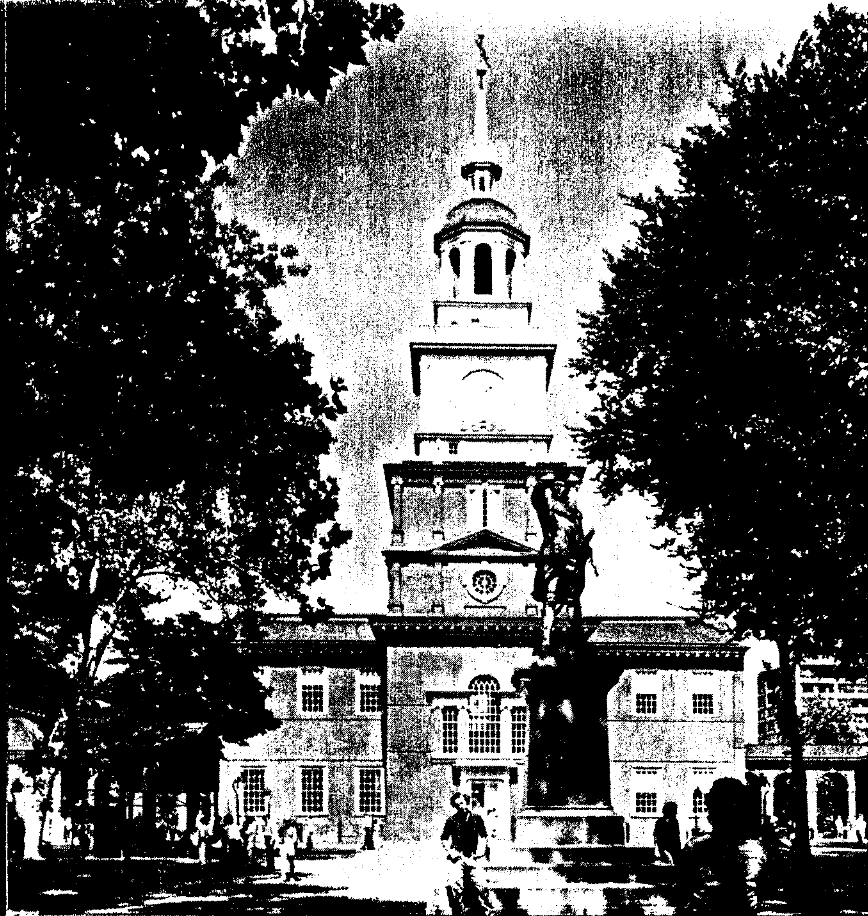

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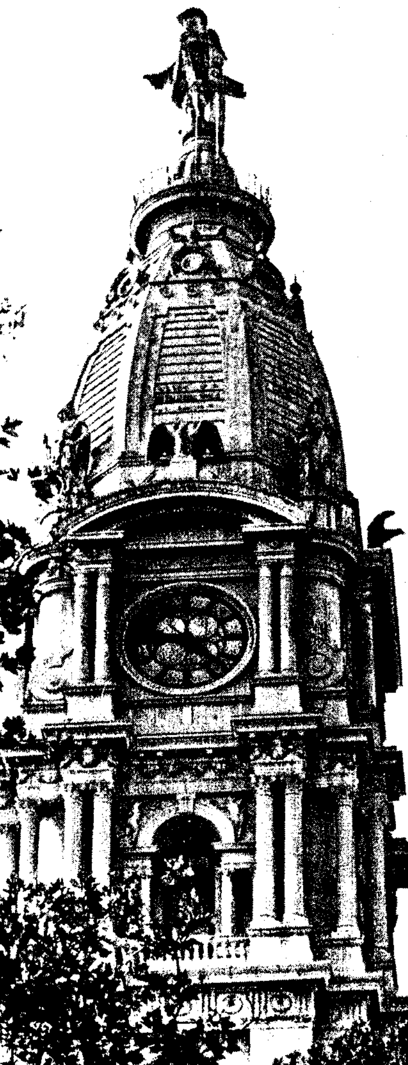

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A DEVICE SIMULATION TOOL FOR HIGH-VOLTAGE BIPOLAR DEVICES

Qiming Wu
François E. Cellier

Dept. of Electrical & Computer Engineering
University of Arizona

ABSTRACT

This paper presents a device simulation tool for high-voltage bipolar devices. This two-dimensional device simulation software package can be used by the design engineer for the optimization of topology and physical parameters of a device in order to increase its breakdown voltage. A variety of applications have indicated that this tool is a versatile, user-friendly, and numerically efficient device simulator. In this paper, some interesting results are shown.

INTRODUCTION

Breakdown voltage is an important parameter in high-voltage devices. In devices manufactured in planar technology, the breakdown usually occurs either on the silicon surface or at the curved junction regions in the bulk. In order to increase the breakdown voltage, the effects of various device parameters such as the doping distribution, the junction depth, and the surface charges, were analyzed, and several topological structures were investigated that are known to raise the breakdown voltage, such as floating diffused rings, floating metal rings and field plates[1,2,3].

Design engineers are interested in maximizing the breakdown voltage of high-voltage devices. For that purpose, they need to know the electric potential and field distributions inside the device. Since no analytic methods exist that allow us to evaluate breakdown phenomena directly, the two-dimensional device simulation is the appropriate technique to analyze the influence of technological parameters and device topology on the breakdown voltage. A two-dimensional device simulation tool for high voltage bipolar devices has been developed for this purpose. This simulator is able to compute all pertinent distributions efficiently and accurately in devices with realistic structures including a variety of materials (Si, SiO_2, Si_3N_4, and Al), and different kinds of topological structures.

In the following sections, we shall describe the physical model used by the simulator. Thereafter, the simulation software package is presented together with some computational results.

PHYSICAL MODEL

In a two-dimensional device simulation, the basic semiconductor equations, i.e. the Poisson equation and the current continuity equations, must be solved. However under high reverse bias voltage on the base-collector junction, the physical model can be simplified. For the analysis of breakdown phenomena, the current in the device can be neglected, and also the emitter can be eliminated, since the collector-base breakdown voltage is the essential phenomenon[4,5]. Therefore, the quasi-Fermi potentials ϕ_n and ϕ_p can be assumed to be constant, and inside the semiconductor, only the Poisson equation needs to be solved.

In order to simulate high-voltage devices realistically, we must take into consideration the regions of insulators, metal electrodes, and also the charges on the surface between semiconductor and insulator.

The normalized equations that are solved by the device simulator together with their corresponding boundary conditions for a typical domain, such as the one shown in *Fig. 1,* are given as

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follows:

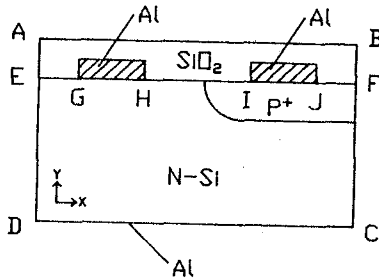

Fig.1: Domain geometry of a typical device

(1) Semiconductor region (Poisson equation):

$$\partial^2\Psi/\partial x^2 + \partial^2\Psi/\partial y^2 = -(\Phi_p \exp(-\Psi) - \Phi_n \exp(\Psi) + N_d) \qquad (1)$$

(2) Insulator region (Laplace equation):

$$\partial^2\Psi/\partial x^2 + \partial^2\Psi/\partial y^2 = 0 \qquad (2)$$

(3) Metal region:

$$\Psi = V_0 \qquad (3)$$

where:

Ψ = static electric potential, unknown variable
$\Phi_n = \exp(-\phi_n)$; ϕ_n = electron quasi-Fermi potential
$\Phi_p = \exp(\phi_p)$; ϕ_p = hole quasi-Fermi potential
N_d = doping concentration
V_0 = known bias voltage

Boundary conditions:

(1) AB: $\partial\Psi/\partial y = 0$ (4)

(2) BC, AD: $\partial\Psi/\partial x = 0$ (5)

(3) EG, HI, JF: $\epsilon_s \partial\Psi/\partial y|_s - \epsilon_i \partial\Psi/\partial y|_i = Q_s$ (6)

where: ϵ_s = permittivity of semiconductor
ϵ_i = permittivity of insulator
Q_S = interface charge density

In the simulator package, the user is allowed to specify devices composed of semiconductor material (Si), insulator materials (SiO_2, Si_3N_4), and metal (Al).

The high-voltage devices fabricated by planar technology usually have two kinds of isolation types: dielectric isolation, and p-n junction isolation. In order to investigate the field distribution of the area in the silicon near the isolation region, the program has been given the ability to simulate devices with a non-rectangular domain.

In practical high-voltage devices, different kinds of floating field rings are employed. In our program, floating diffused rings or floating metal rings can also be simulated.

SOFTWARE PACKAGE STRUCTURE

The device simulation software package includes graphical input of the device topology, input of the physical device parameters, numerical solution of the basic semiconductor equations, and numerical as well as graphical output of the computational results. The overall hardware/software structure of the system is presented in *Fig.2*.

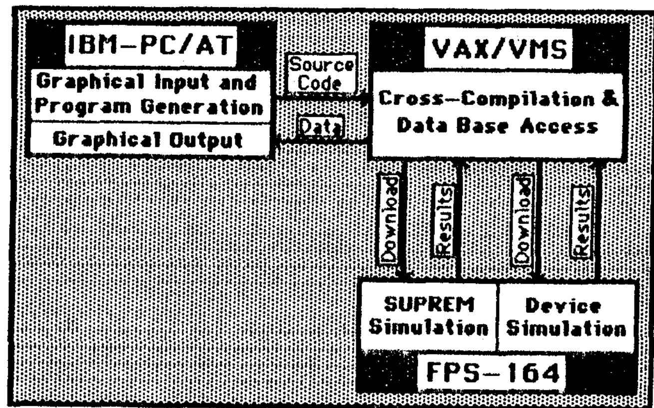

Fig.2: Overall hardware/software system structure

The software package has a user-interface which is convenient to use and yet flexible. Users can design device topologies graphically on a PC-class machine which then generates the device simulation source code to be downloaded to a VAX/VMS system. The VAX is responsible for cross-compilation of the device simulation program for further processing by an array processor. The FPS-164 array processor performs the actual simulation about 6 times faster than the VAX. Simulation results are then shipped back to the VAX for storage in the VAX-maintained data base. From there, any data can be called back by the (portable) graphical postprocessor that can either reside on the IBM-PC or on the VAX.

For the device simulation, several physical parameters such as doping concentration, surface charge, and bias voltage are needed. While some of these data are user-generated, the doping concentration is automatically extracted from the output file of a SUPREM-III simulation run[6]. It is then stored in a relational data base from where it can be fetched any time for use by the device simulation program. A special program translates one-dimensional doping distributions into two-dimensional doping distributions.

After comparing different numerical algorithms, a finite difference method was used to discretize the elliptic PDE's, a Newton iteration scheme was used to linearize the resulting non-linear algebraic equations, and the finally obtained linear algebraic equations are solved by use of two ELLPACK modules - MINIMUM DEGREE and SPARSE GE NO PIVOTING which required the least computation time and storage. ELLPACK[7] is a powerful software system for solving elliptic boundary value problems. It was initially used by us to identify the most appropriate solution techniques[8]. The MINIMUM DEGREE module computes an indexing scheme which attempts to minimize the number of non-zero elements of the resulting sparse coefficient matrix of equations. The SPARSE GE NO PIVOTING module solves the sparse system of linear equations by using sparse Gaussian elimination without pivoting.

Our device simulation program automatically generates the discretization grid. A non-uniform grid is generated according to the boundaries of the different regions and the gradient of the doping concentration in the device.

The graphical postprocessor is an interactive program specially designed for representation of simulation data residing in a relational data base. It contains its own GKS kernel with a very flexible terminal driver interface.

The application data base is a relational data base also specialized for holding data stemming from technical applications. All the input and output data are maintained in the data base including device topology data, physical parameters, doping concentrations extracted from the output of a SUPREM-III simulation, and the result data of the device simulation itself. Every program in the program suite has an interface to the relational data base for communication with the rest of the software.

After carefully selecting the numerical algorithms and organizing the program and by use of the array processor (FPS-164) hooked to a VAX-11/750 for speed-up purposes, we were able to reduce the execution time of the device simulation program from initially several hours to a few minutes for a device with 100+400 Volts reverse bias voltage on the p-n junction.

COMPUTATIONAL RESULTS

The investigation of high reverse voltage planar semiconductor devices has been described in several papers[1,2,3,4,5,9]. In these papers, it has been discussed how physical parameters of the semiconductor, such as its doping concentration, the main junction depth, surface charges, field plates with non-uniform oxide thickness, floating diffused rings or floating metal rings influence the field distribution and breakdown voltage. Optimal combinations of device parameters are suggested that help to increase the breakdown voltage.

We simulated several such devices in order to investigate how the device structure influences the electric potential and field distribution. Thereby, the device surface topology was kept as close to reality as possible. In the following examples, the doping concentrations were taken from SUPREM-III process simulation results.

1. In *Fig.3*, two simulation device structures are shown. In *Fig.3(a)*, the p-region electrode is lengthened to cover the p-n junction. This electrode extends to the left and forms a field plate. In *Fig.3(b)*, the p-region electrode is shorter, and the field plate is eliminated. The p-region and the bottom of the silicon are grounded. A reverse bias voltage of 200 Volts is applied to the p-n junction. The computational results have shown that the field plate causes the field distribution to change, and the equi-potential lines to move to the left, so that the electric field intensity near the p-n junction curvature and the surface is indeed reduced. By removing the field plate, the highest field value grows from *250 kV/cm* to *284 kV/cm*, and the highest field point moves from the surface of the silicon to the p-n junction curvature.

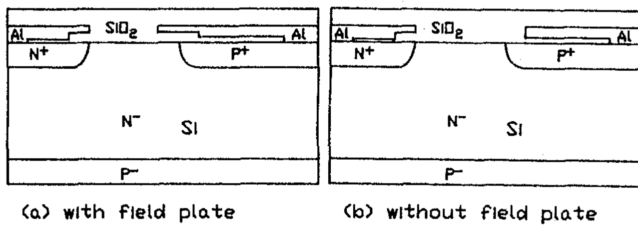

Fig.3: Device structure with and without field plate

2. In order to investigate the region near the p–n junction isolation area, the region shown in *Fig.4* has been simulated. Here, a high voltage (100V) Al electrode covers the p–n junction. The left side and the bottom of the silicon are grounded. Through the SiO_2 layer, the high reverse bias voltage of the electrode directly influences the highest field location on the surface of the p–n junction high resistance area. The thickness of the SiO_2 layer t_{ox} influences the value of the highest field. In *Fig.5*, the highest electric field intensity E_{max} is graphed *vs* the oxide thickness t_{ox}. A thicker oxide layer helps to reduce the maximum field value in the silicon.

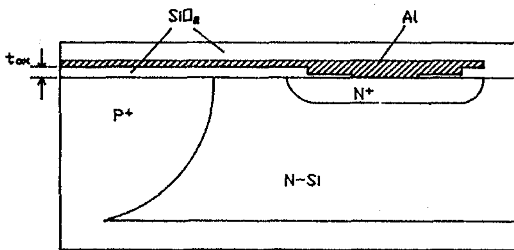

Fig.4: Structure of the region near the p–n junction isolation

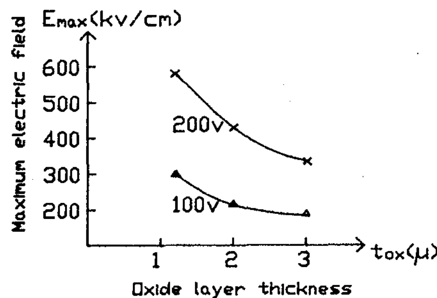

Fig.5: The highest electric field intensity E_{max} plotted *vs* the oxide thickness t_{ox}

3. In order to investigate the influence of floating rings, the same device was simulated once with and once without a floating diffused ring. The p–region and the bottom of the silicon were grounded. A reverse bias voltage of 200 Volts was applied to the p–n junction. Results of these simulations are presented in *Fig.6(a)* and *Fig.6(b)*. Due to the existence of the floating ring, the equi–potential lines move towards the high reverse bias electrode contact region. The resulting electric field shows that the highest field point is no longer located on the p–n junction curvature, and that the field near the p–n junction has been reduced.

CONCLUSIONS

The computational results obtained have shown that our device simulation program can both efficiently and reliably be used to simulate different kinds of high–voltage devices. Since the program allows the devices to consist of several different materials with arbitrary (rectangular) shapes, it is sufficiently flexible for simulation of a large variety of different industrial high–voltage devices. Using this program, the comparison between several different layouts of device structures is made easy.

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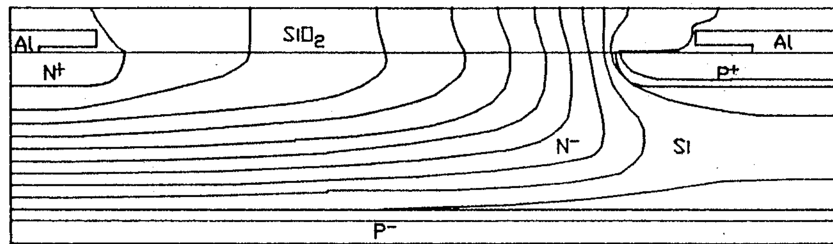
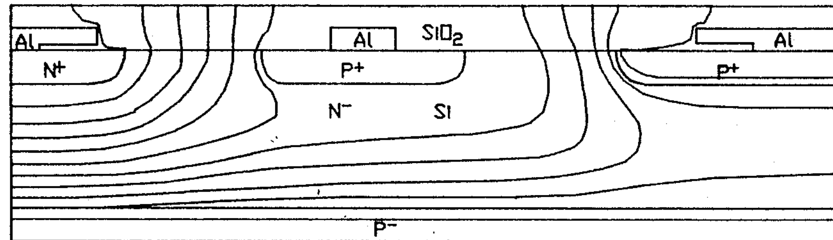


(a) without floating diffused ring



(b) with floating diffused ring

Fig.6: Contour plot of the electric potential distribution of a device with and without floating diffused ring