OPTIMIZATION OF A TWO-LEVEL FIELD-PLATE TERMINATION STRUCTURE FOR INTEGRATED-POWER APPLICATIONS IN IONIZING RADIATION ENVIRONMENTS

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Abstract

Analysis of four two-level field plate (FP) termination structures for power-integrated circuit applications in ionizing radiation environments has been performed through two-dimensional simulation and experiment. Breakdown voltage degradation as a function of the distance the upper plate overlaps the lower plate was obtained. Optimization of the upper plate overlap with respect to device area and radiation hardness was accomplished.

I. Introduction

Termination structures are employed by power semiconductor devices to increase their drain-source breakdown voltage to near the ideal, or parallel-plane value, which is set by the doping of the lightly-doped epitaxial region.[1] A cross-section of a typical integrated power DMOS device, showing two cells, is shown in figure 1. The termination region lies around the periphery of the cells.

In general, n-channel power-device breakdown voltage degrades with increasing radiation-induced positive trapped charge, N_{ot}.[2] Thus, a termination structure for power devices in radiation environments must meet its breakdown specification for increasing values of N_{ot}. The two most frequently used termination methods are field plates (FPs) and field-limiting rings (FLRs). Although FLRs, when properly placed, can provide excellent radiation immunity,[2] they must be diffused very accurately for optimum performance.[3,4] FP termination structures, on the other hand, do not require such precise photolithographic control, and may even require less area than FLR designs for the same breakdown voltage in some cases. These and other processing considerations may make FPs an attractive alternative to FLRs.

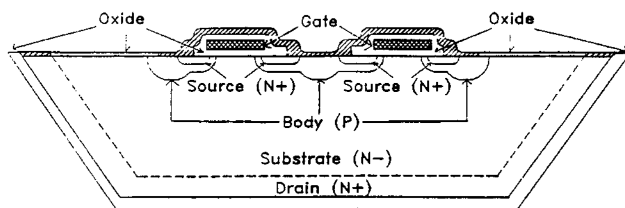


Figure 1. Representative cross-section of a power integrated DMOS device showing two cells.

The operation of an FP termination structure can be understood in terms of simple electrostatics. An FP induces charges in the semiconductor that effectively extend the junction they are terminating. In general, the more charges that an FP can induce in the semiconductor for a given voltage, the more effective the FP will be in raising the breakdown voltage. The charge induced by the FP is, of course, a strong function of oxide thickness under the FP. In n-channel devices, N_{ot} offsets some of the plate-induced charge, which translates directly into breakdown voltage degradation. In p-channel devices, N_{ot} enhances the plate-induced charge, which can lead to breakdown voltage enhancement.[5]

The maximum breakdown voltage for FP termination structures has been given as a function of oxide thickness for relatively low substrate doping.[6] However, in power-integrated circuit (PIC) devices, lower device voltage ratings are typical, which implies more heavily doped substrates. In this case, accurate prediction of the breakdown voltage can only be accomplished with two-dimensional simulation.

The breakdown voltage degradation of otherwise identical power DMOS devices with different two-level FP structures as a function of total ionizing dose was investigated. It was found that an upper field plate reduces the degradation somewhat. Also, an upper bound for the upper-plate overlap, beyond which no significant improvement in hardness results, was obtained. This distance defines the optimum upper-plate overlap, which is essential to minimizing device area.

II. Two-Dimensional Simulation

A. Method

Computer code designed to simulate the effects of ionizing radiation on the breakdown voltage of power semiconductor devices has been developed at the University of Arizona.[2] The code, entitled ASEPS (Arizona SEmiconductor Power device Simulator), solves Poisson's equation in two dimensions. Breakdown voltage is then determined by computing the ionization integral through the locus of highest-field points at every potential. ASEPS has proven to be an accurate and efficient simulator of highly reverse-biased junctions with arbitrary termination topologies and N_{ot}.[2] Its flexible input format enables comprehensive study of competing termination designs.

B. Parameters

The DMOS devices studied were all n-channel devices with a maximum achievable breakdown voltage of approximately 270 *V* (parallel-plane junction limit). All had a lower FP of fixed length (6.5 μm) and fixed oxide thickness (0.86 μm). The devices had upper-plate overlaps of either 0, 5, 10, or 15 μm and oxide thicknesses approximately three times greater than the oxide under the lower plate. A qualitative cross-section of the termination region of these devices is shown in figure 2.

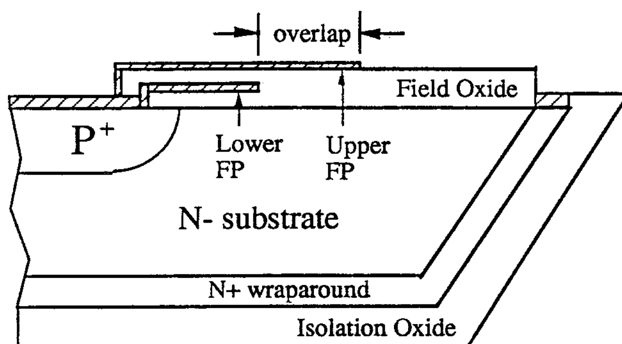


Figure 2. Cross section of the termination region of the devices in the text. A two-level FP termination structure is shown over the drain-body junction.

C. Modelling

ASEPS was used to gain insight into the effects of the upper field plate on breakdown voltage degradation. However, several considerations are necessary to obtain simulation results that accurately reflect experimental conditions. To do a completely accurate prediction of breakdown voltage degradation, ASEPS requires the equivalent charge at the Si-SiO_2 interface under the FP as a function of total iozing dose. This charge is taken to be constant with lateral position.

This mapping is difficult to obtain because, in general, reverse biasing the power device at, say, 100 *V* does not mean that the entire 100 *V* is dropped across the oxide under the FP, especially for low total dose. In fact, the electric field across the oxide under the FP depends on such things as substrate doping, oxide thickness under the FP, and N_{ot}. These variables are difficult to account for in a tractable test setup. Furthermore, since the electric field under the FP varies with lateral position, N_{ot} buildup under the field plate also varies with position. However, simulation can still be used to acquire insight into the breakdown performance of the devices under study.

To calibrate the simulations, simulation results were fit to experimental breakdown voltage versus total dose data for the device with 0 μm upper-plate overlap. Then the devices with 5, 10, and 15 μm overlap were simulated with the same values of N_{ot} as were used in the calibration. ASEPS output for three of these four devices are presented in figure 3. In these figures, the lines are equipotential lines, and the circles indicate highest electric-field points. A constant value of $N_{ot} = 7 \times 10^{11}\ cm^{-2}$ is assumed for all devices. This is the maximum equivalent value of N_{ot} ($N_{ot,max}$) under the FP, as explained in section III. It can be seen that the charges induced by the upper field plate in the semiconductor expand the equipotential lines, reducing the breakdown voltage degradation.

III. Experimental Results

The four device types (having different termination structures) were irradiated in a Co-60 source (dose rate approximately 20 *rad(Si)/min*) under constant reverse-bias voltage of 100 *V* to a total dose of nearly 150 *krad(Si)*. The

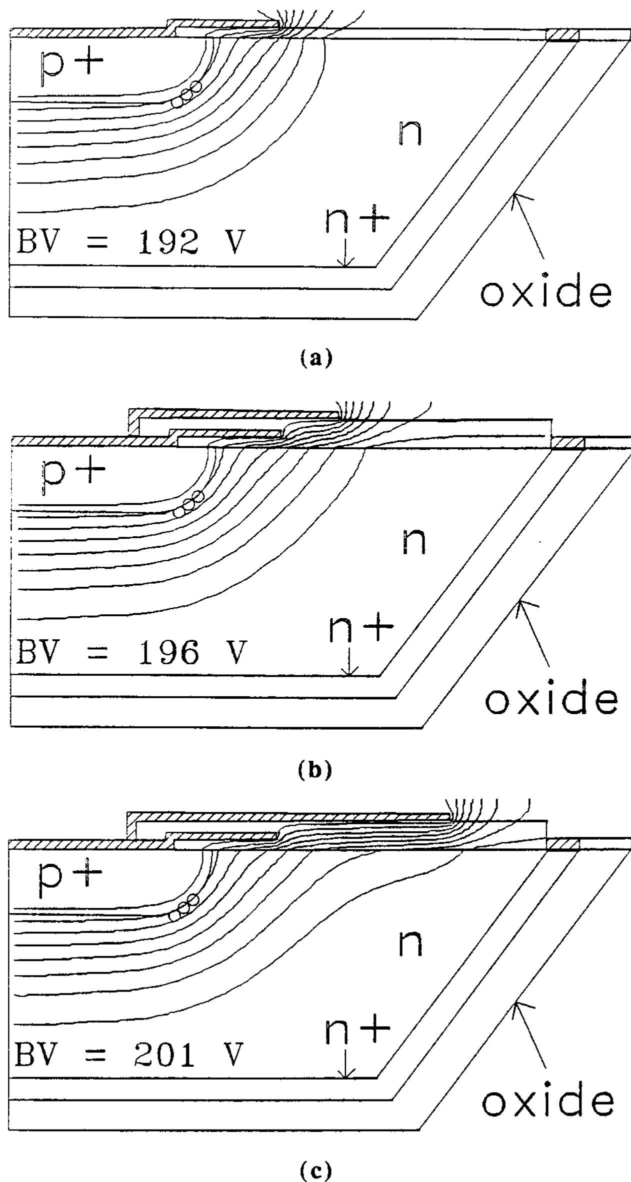
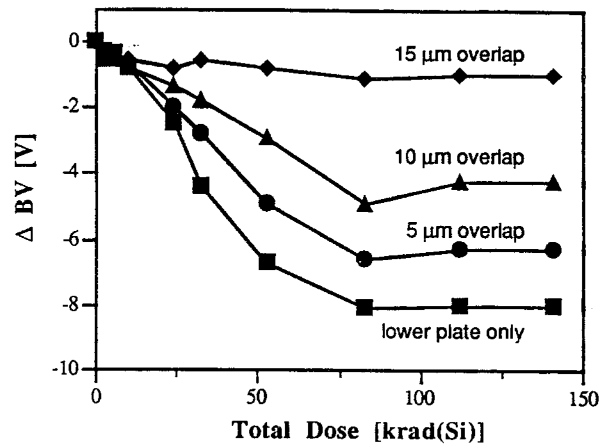


Figure 3. ASEPS simulation results showing the effect of increasing upper-plate overlap. $N_{ot} = N_{ot,sat} = 7.0 \times 10^{11}\ cm^{-2}$ is present in all devices. a) Lower plate only. b) 5 μm upper-plate overlap. c) 15 μm upper-plate overlap.

bias mimics the normal operating mode of the device in a typical circuit application. Breakdown voltage was taken to be the reverse-bias drain-source voltage that gave 1 *mA* of leakage current. The breakdown voltage of all devices, even the device with no upper FP, did not degrade beyond a total dose of 75 *krad(Si)*; this implies that N_{ot} buildup saturated beyond 75 *krad(Si)*.

Worst-case experimental results are compared with simulation results in figure 4. The use of a hardened field oxide resulted in all devices tested having excellent resistance to breakdown degradation. In figure 4a, (worst-case) experimental breakdown voltage degradation, ΔBV, versus



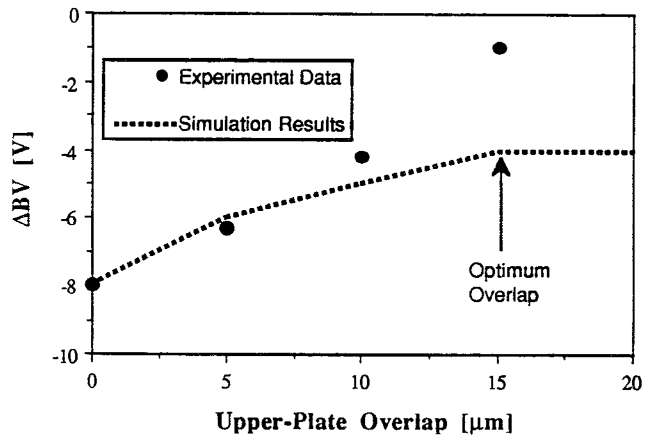


Figure 4. Comparison of ASEPS simulation results and experimental data. a) Experimental breakdown-voltage degradation as a function of total dose for the four devices discussed in the text. b) Change in breakdown voltage at 75 *krad(Si)* as a function of upper-plate overlap. The optimal overlap is identified as the overlap at which no improvement in hardness would result by increasing the overlap.

plate length is shown. This data can be used to calibrate the ASEPS simulation results. If a linear relationship between total dose and N_{ot} is assumed for the range 0 - 75 *krad(Si)*, a reasonable first-order model of N_{ot} buildup under the FP is obtained. N_{ot} is fixed, or saturated, at $N_{ot,sat}$ for all total doses beyond 75 *krad(Si)*, in accordance with the experimental data.

ΔBV is plotted versus upper plate overlap in figure 4b. The experimental data are taken for doses at or beyond 75 *krad(Si)*; accordingly, the simulation results assume $N_{ot} = N_{ot,sat} = 7.0 \times 10^{11}\ cm^{-2}$. In both figures, ΔBV, is plotted instead of absolute voltage so that chip-to-chip variations in initial breakdown voltage do not skew the comparison. All absolute voltages measured, however, were in the range 190 - 210 *V*, in agreement with simulation results. It can be seen that the optimum upper plate overlap is 15 μm, since further increases in upper-plate overlap would provide minimal additional hardness. If the degradation of the device with 0 μm upper-plate overlap can be tolerated, substantial savings in device area are possible.

IV. Conclusion

The breakdown-voltage degradation of an integrated-power DMOS device with several different termination structures was studied both experimentally and through two-dimensional simulation. It was shown that the presence of an upper field plate enhances the radiation hardness of the device, and that an optimal overlap can be predicted by simulation.

V. References

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