TWO-DIMENSIONAL SIMULATION OF THE EFFECTS OF TOTAL DOSE IONIZING RADIATION ON POWER-MOSFET BREAKDOWN

by

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ABSTRACT

The effects of ionizing radiation on the breakdown–voltage degradation of power–MOSFET termination structures were examined through two–dimensional simulation. A wide variety of sensitivity to surface–charge density was found for various devices employing floating field rings and/or equipotential field plates. Termination structures that were both insensitive to surface charge and possessed a high breakdown voltage were identified. The results were compared with measurements made on selected structures.

The principal ionizing radiation damaging mechanisms in MOS devices are discussed. Modifications made to an existing simulation program in order to simulate these complex field ring and field plate structures are described. Background information into how these termination structures improve the breakdown voltage and their sensitivities to positive interface charge buildup is investigated.

CHAPTER 1
INTRODUCTION

The maximum breakdown voltage obtainable for a *p-n* junction of specified doping concentration occurs for a planar structure [9]. In actual devices utilizing planar diffusion technology, however, the high–voltage junction must intersect the surface at some finite position. The resulting junction curvature compresses the equipotential lines where the junction bends to the surface and increases the peak electric field. Junction termination structures are used in power devices to reduce the peak electric field and to allow the breakdown voltage to approach its ideal planar junction value. The term "junction termination structure" is thus defined as the manner in which the metallurgical junction is terminated at the surface of a semiconductor device. The most commonly used termination methods for power MOSFETs (metal–oxide–semiconductor field–effect transistors) are floating field rings and equipotential field plates. Fig. (1-1) shows the cross–section of a typical power MOSFET with one floating field ring.

Avalanche multiplication is the physical mechanism that causes the primary breakdown of high–voltage reverse–biased *p-n* junctions. Breakdown occurs when the electric field in the junction depletion region increases to the point at which the impact ionization rate approaches infinity. The most important factor that influences the magnitude and location of the peak electric field in planar semiconductor technology is the method used to terminate the junction [9,10,11]. The objective of the different termination methods is to reduce the peak electric field either at the surface or at the curved junction regions in the bulk.

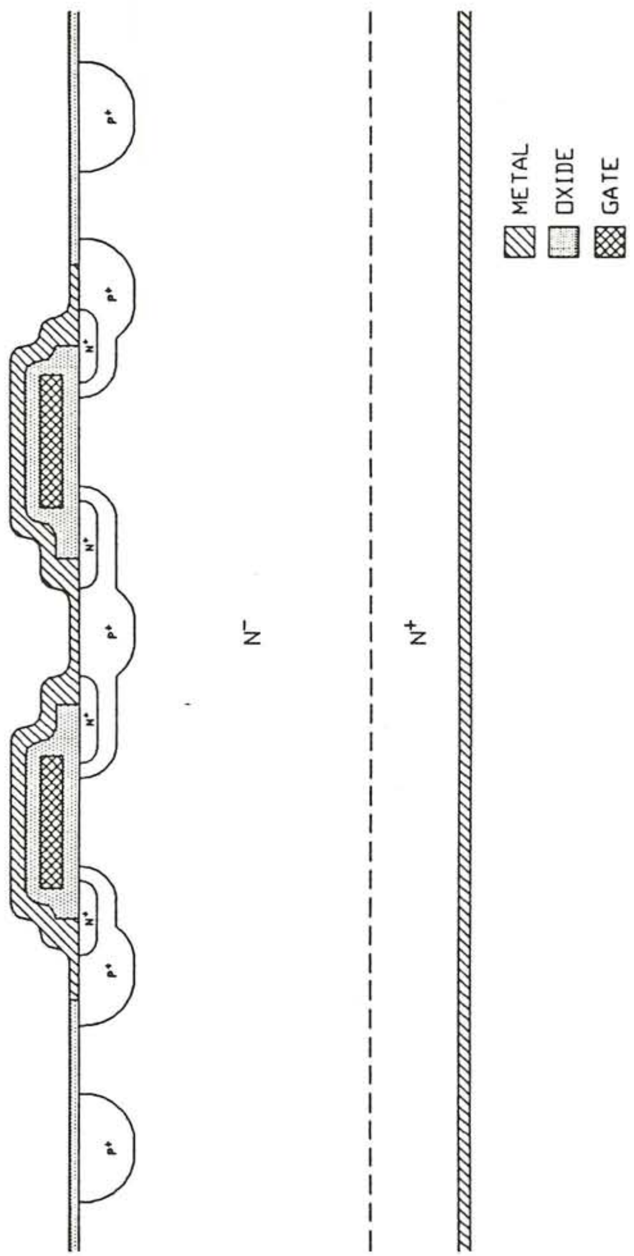


Figure 1-1. Cross–section of power–MOSFET with one floating field ring.

The drain–source breakdown voltage of power–MOSFETs is strongly affected by ionizing radiation [13,38]. This effect is a result of the introduction of trapped oxide and interface charge in the field oxide. In this work, positive charge build up is assumed to be the algebraic difference between the positive oxide trapped charge (N_{ot}) and the negative interface trapped charge (N_{it}). These trapped charges alter the potential at the surface of the junction and, in turn, become a part of the junction termination. Therefore, radiation–induced charge affects the breakdown voltage of high–voltage junctions.

Power MOSFETs are desirable for electronic systems for applications in space environments because of their reduced drive power requirements, low mass, and short switching times [8]. It is desired that a satellite stay operational as long as possible, but being subjected to ionizing radiation in space limits the life of the satellite. A synchronous satellite accumulates an extremely high radiation dose during its 7– to 10–year lifetime. Although the radiation received by a given component is reduced by shielding effects of the spacecraft structure and the equipment enclosure, it will still be subjected to about 10^5 rads (see Chapter 2) in most locations. This amount of radiation is sufficient to damage most components. Therefore, it is desired to continually improve components such that they are able to tolerate higher levels of radiation.

This paper reports on work designed to examine the effects of ionizing radiation on commonly used power–MOSFET termination structures. Simulations were conducted using computer code specifically designed for this purpose. In Chapter 2, sources and environments of ionizing radiation are described. In addition, the damaging effects of this radiation on semiconductor devices are introduced. Definitions of total dose and dose rates used to describe ionizing radiation exposure are presented. Chapter 3 illustrates the physics of semiconductor breakdown caused by

high reverse–bias voltages. The impact ionization process and ionization integral are explored. Chapter 4 describes an existing simulation program and modifications that were necessary to perform ionizing radiation simulations on selected termination structures. In Chapter 5, termination structures are described in some detail. The means in which termination structures improve breakdown voltage and avoid effects of charge buildup are the main concern. In Chapter 6, results of simulations are presented and are compared with measurements made on selected structures. Qualitative explanations of the observed outcomes are discussed. Insights into the design of optimum termination structures are obtained. In Chapter 7, a function to determine punch–through voltage between rings of a floating filed ring structure is presented. The three variables used in this function are ring spacing, surface–charge density, and background (surface) doping concentration.

CHAPTER 2
RADIATION ENVIRONMENTS

There are four main types of radiation environments. These include neutrons, energetic heavy ionized particles, total–dose ionizing radiation, and dose–rate (gamma dot) ionizing radiation. Neutrons are not considered as ionizing radiation, but the other three types are. All of these types of radiation can cause displacement damage in the lattice of the incident material, but the dominant effect of ionizing radiation is the creation of electron–hole pairs.

Ionizing radiation is produced naturally in space. Also, man–made sources of radiation include nuclear explosions, nuclear reactors, and integrated circuit processing. Exposure of power MOSFETs to total–dose ionizing radiation causes degradation in breakdown voltage, transconductance, and leakage current, but the dominant effect is the large shift in threshold voltage. This work is concerned with the degradation of breakdown voltage caused by ionizing radiation. Ionizing radiation deposits energy in materials measured in terms of the rad (radiation absorbed dose). One rad is defined as the absorption of 100 ergs per gram of energy by the material (1 erg $= 10^{-7}$ J).

Although radiation can have a number of effects on a device, this work is directed to the investigation of ionizing radiation effects on the high–voltage junction termination of power MOSFETs. The primary portions of the termination structures affected by adiation are the field oxide and the interface between the silicon and silicon dioxide.

2.1 Ionizing Radiation

Ionizing radiation produces electron–hole pairs in the silicon dioxide. Once generated, the pair may be separated due to the field in the oxide. The electron moves relatively quickly to a metal conductor while the hole makes its way slowly to the silicon. The hole may become trapped at the Si–SiO_2 interface which is referred to as positive charge buildup. Ionizing radiation also creates new states at the interface, and charge exchange between these states and the silicon takes place in response to Fermi level changes.

Figure (2-1) shows, in simplified form, the steps that occur in the charge buildup process in an MOS device gate oxide for n–type silicon. In (a), the device is in an equilibrium state. In (b), the ionizing radiation creates electron–hole pairs throughout the oxide. Immediately after pair formation, recombination and electron transport occur simultaneously. Some electron–hole pairs will recombine while some electrons will reach the metal as shown in (c). Electron mobility in SiO_2 at room temperature is approximately $20\,cm^2/V\text{-}sec$ which is much larger than the hole mobility, $2 \times 10^{-5}\,cm^2/V\text{-}sec$. Thus, the electrons that escape the initial recombination reach the metal in picoseconds, leaving behind immobile holes (d). In the field oxide, these electrons travel horizontally toward the source or drain metal electrodes. Holes begin to migrate relatively slowly to the oxide–semiconductor interface (e). Some holes become trapped at the interface while the remainder pass into the silicon. Figure (f) shows the stable condition after hole transport has completed, resulting in positive charge buildup.

The percentage of generated holes that become trapped can range from 1% for hardened oxides to 30% or more for unhardened oxides [46]. Electron trapping in the oxide is negligible compared to the number of holes trapped. Also important

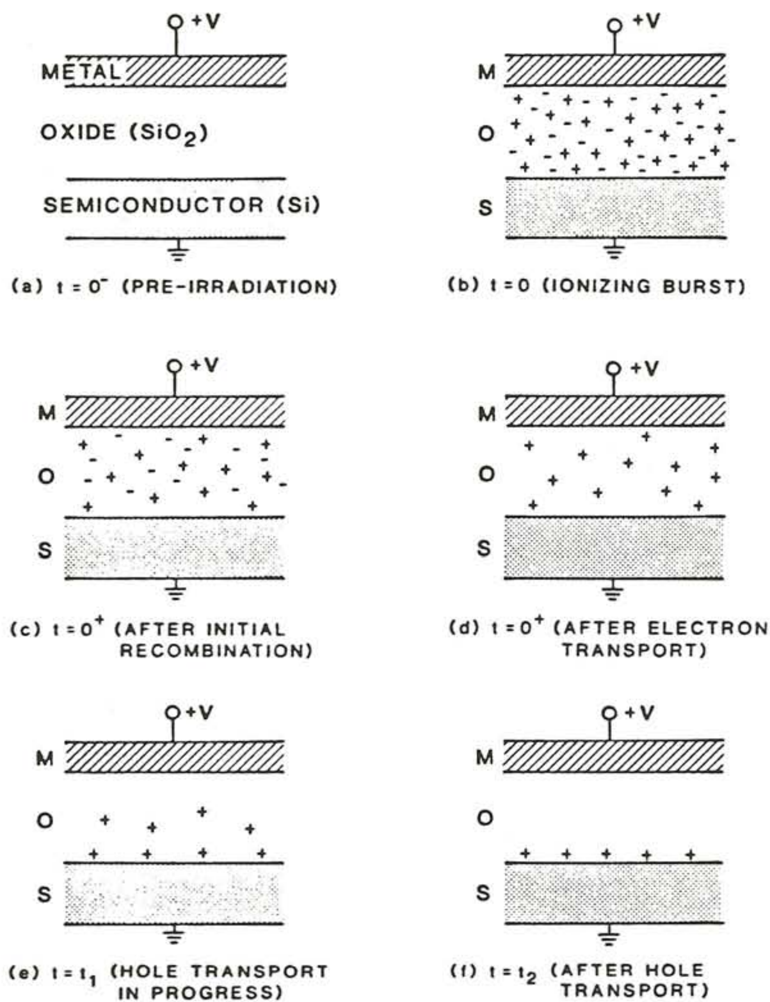


Figure 2-1. Positive charge buildup process in an SiO_2 layer. This includes recombination, transport and trapping of carriers. (After Srour [46].)

is the fraction of electron–hole pairs that escape initial recombination. As the electric field in the oxide increases, so does the number of escaped pairs. Lower temperatures result in more trapped holes because of the hole's decreased mobility.

Experiments have shown that the average energy required of incident photons to produce an electron–hole pair is $3.6\,eV$ in silicon and $2.8\,eV$ in germanium $(1eV = 1.6021 \times 10^{-19}\,J)$. The carrier generation constant, G, for silicon can then be determined to be 4.2×10^{13} electron–hole pairs per cm^3–rad(Si) [31]. This value comes from:

$$(1\,e{-}h\,pair\,per\,3.6\,eV) \cdot (100\,ergs/g\,per\,1\,rad(Si)) \cdot (2.42\,g\,Si\,per\,cm^3) \cdot$$

$$(1\,eV\,per\,1.6021 \times 10^{-12}\,ergs). \qquad (2-1)$$

In this work, it was necessary to give some correlation between a rad of radiation and positive charge buildup at the surface. As was mentioned in the previous section, the percentage of generated holes that become trapped is a function of the type of oxide used. From McGarrity [33], the total dose can be converted to the density of oxide trapped charge near the interface using the formula,

$$N_{ss} = D\,t_{ox}\,G\,F \qquad (2-2)$$

where D is the total dose, t_{ox} is the oxide thickness, G is the generation rate of electron-hole pairs per unit volume, and F is the fraction of holes transported and trapped at the interface. For silicon dioxide, the generation constant G is 7.5×10^{15} electron–hole pairs per cm^3–krad [34]. For the different structures being simulated, an appropriate F factor can yield the conversion desired. The use of a hardened field oxide or reducing the oxide thickness will reduce the amount of charge buildup as a function of total dose. The radiation-induced surface-charge density, N_{ss},

is an input parameter to the computer code used. In this work, N_{ss} represents the algebraic difference between the positive oxide trapped charge (N_{ot}) and the negative interface trapped charge (N_{it}) and is taken to be positive.

CHAPTER 3
BREAKDOWN

One of the most important characteristics of a power semiconductor device is the breakdown voltage [11]. This parameter, along with the maximum current handling capability, determines the power rating of the device. The breakdown voltage is the maximum voltage that may be applied between the drain and source of MOSFETs and the reverse–bias voltage for most *p-n* junction diodes. Applications of power devices require voltages ranging from $25\,V$ to $6000\,V$. In an MOS device, the voltage is supported by a depletion layer formed adjacent to the chain–body junction creating a high electric field. This field is responsible for sweeping out any holes or electrons that enter this region, either by the process of space–charge generation or diffusion from the neighboring quasi–neutral areas. The electric field increases as more reverse–biasing voltage is applied across the depletion layer which then accelerates mobile carriers to higher drift velocities. Eventually, a point is reached when mobile carriers attain their terminal drift velocity ($10^7\,cm/sec$ for electrons and $6.5 \times 10^6\,cm/sec$ for holes in silicon) [26].

With further increase of electric field, the velocity of these individual carriers exceeds their thermal velocity and they become "hot" carriers. At higher electric fields, these carriers have enough energy in their collisions with atoms in the lattice to excite valence band electrons into the conduction band. Impact ionization is the name of this process for the generation of electron–hole pairs. These newly created electron–hole pairs exist in the same electric field and are accelerated to participate in the creation of further electron–hole pairs. Impact ionization thus

causes a surge of mobile carriers to be transported through the depletion layer. This cumulative process is referred to as avalanche multiplication. Avalanche multiplication is the physical mechanism that causes the primary breakdown of high–voltage reverse–biased *p-n* junctions [61]. The device is recognized to experience avalanche breakdown when the rate of impact ionization approaches infinity because it can no longer tolerate an increase in applied voltage. Avalanche breakdown limits the operating voltage of power devices.

In this chapter, the derivation of the basic ionization integral that describes breakdown is investigated. The physics involved in this avalanche breakdown process is analyzed. Insights into different types of junctions and terminations and why they have separate breakdown voltages are covered.

3.1 Avalanche Breakdown

Reverse–biased silicon *p-n* junctions at room temperature display an extremely small leakage current [61]. Hence, for many purposes, a reverse–biased junction can be modeled as an open circuit. However, for a majority of junctions, there exists a critical voltage where reverse current begins to increase sharply with increases in voltage. This voltage is known as breakdown voltage.

Avalanche breakdown is defined as the condition under which the impact ionization process attains an infinite rate. Impact ionization occurs generating electron–hole pairs during the transport of mobile carriers through the depletion layer. The electron–hole pair generation rate G from impact ionization is given by [52]

$$G = \alpha_n \, n \, v_n + \alpha_p \, p \, v_p \qquad (3-1)$$

where α_n and α_p are the ionization rates of electrons and holes, respectively. Also, n and p are the carrier concentrations, and v_n and v_p are the drift velocities.

3.1.1 Ionization Coefficients

To characterize the impact ionization process, the avalanche-breakdown theory must first begin with a study of the ionization coefficients (rates) for electrons and holes. These coefficients represent the ability of energetic electrons and holes to produce additional carriers in pairs. The impact ionization coefficient for electrons (α_n), which has units of cm^{-1}, is defined as the number of electron–hole pairs created by one electron traveling $1\,cm$ in the direction of the electric field through the depletion layer. The rate for holes (α_p) is defined similarly, but for one hole traveling $1\,cm$.

Both α_n and α_p depend greatly on the electric field E. Extensive measurements on these ionization rates for silicon have been conducted [50,57] indicating that they are of the form

$$\alpha_{n,p} = a\,exp(-b/|E|) \qquad (3-2)$$

where E is in V/cm. A comparison of the approximate values of these coefficients for silicon from two research teams are given in Table 3-1.

Table 3-1. Comparison of ionization coefficients from two research teams.

Comparison of *a* and *b* coefficients in ionization rate expressions		
	Sze and Gibbons [50]	Van Overstraeten, *et al* [57]
a for electrons	$3.8 \times 10^6\,cm^{-1}$	$7.03 \times 10^5\,cm^{-1}$
b for electrons	$1.75 \times 10^6\,V/cm$	$1.231 \times 10^6\,V/cm$
a for holes	$2.25 \times 10^7\,cm^{-1}$	$1.582 \times 10^6\,cm^{-1}$
b for holes	$3.26 \times 10^6\,V/cm$	$2.036 \times 10^6\,V/cm$

Eq. (3-2) applies for electric fields ranging from 1.75×10^5 to $6.0 \times 10^5\, V/cm$. α_n and α_p are plotted as functions of the electric field E in Fig. (3-1). There is an extremely rapid increase in the impact ionization coefficients with increasing electric field which is very important to note for the analysis of breakdown in power devices.

Fulop [25] found that it is possible to combine the electron and hole coefficients into one equation that could fit the experimental data. For silicon, these coefficients are: $a = 9.0 \times 10^5\, cm^{-1}$ and $b = 1.8 \times 10^6\, V/cm$. For device design calculations, reducing this equation to the following form has given very useful results [25]

$$\alpha_{eff} = c\, exp(|E|^g)\, cm^{-1}. \qquad (3-3)$$

For silicon $c = 1.8 \times 10^{-35}$, $g = 7$, and E is in V/cm. This approximation allows closed–form solutions to the avalanche breakdown voltage of abrupt junctions as well as for cylindrical and spherical junction terminations. This approximation is compared to the more accurate expressions in Fig. (3-1).

3.1.2 Ionization Integral

Once expressions for α_n and α_p are known, the next step is to calculate the condition for avalanche breakdown. In Fig. (3-2), the depletion region for a strongly reverse–biased np^+ junction is shown [36]. Almost all of this region will lie in the n–type material because of its considerably lower impurity concentration. At the left–hand boundary where $x = 0$, the incident hole current $I_p(0)$ is a very small component of the total current because holes are the minority carriers at that location. At the right–hand boundary where $x = W$, the hole component $I_p(W)$ is essentially equal to the total current I. This is true because this boundary lies in the p^+ region of the np^+ junction.

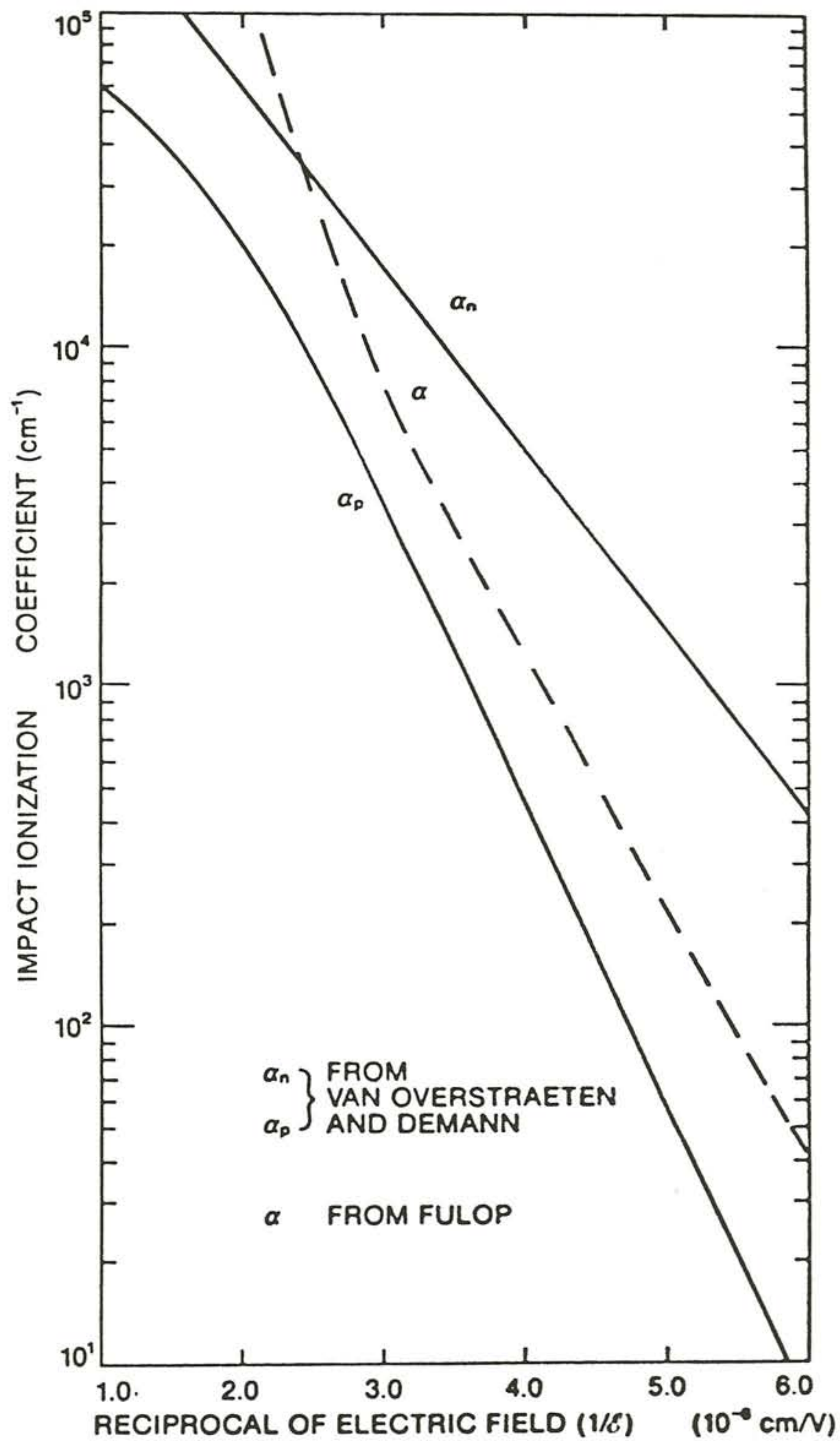


Figure 3-1. Impact ionization coefficients in silicon. (After Baliga [11].)

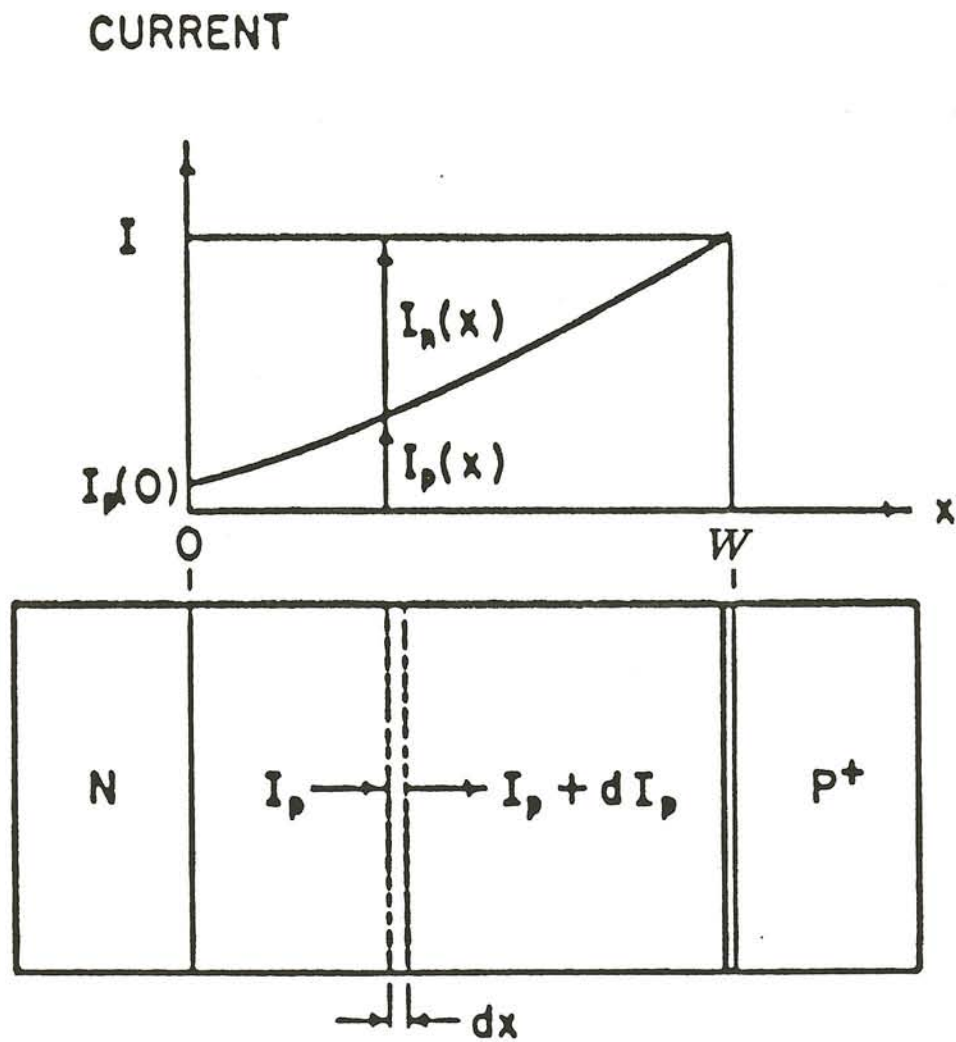


Figure 3-2. Schematic diagram of hole and electron currents in an np^+ junction depletion region and multiplication of incident current. (After Moll [36].)

At a distance x into the depletion region, the hole–current increase is caused by the generation of electron–hole pairs. The hole and electron currents are

$$I_p(x) = q\,A\,p\,v_p \tag{3-4}$$

and

$$I_n(x) = q\,A\,n\,v_n. \tag{3-5}$$

In Eq. (3-4) and Eq. (3-5), q is the elementary charge and A is the junction area. In the infinitesimally small layer dx, additional holes are produced by the impact ionization of both holes and electrons. This leads to the hole–current increment dI_p being written as

$$dI_p = \alpha_p\,I_p\,dx + \alpha_n\,I_n\,dx. \tag{3-6}$$

Because of the choice of orientation in Fig. (3-2), this hole–current increment is positive in the positive x direction. The hole current changes by an amount equal to the number of electron–hole pairs generated per second in the dx layer (times the electronic charge).

Electrons are produced by the impact ionization process in the dx layer at the same rate as holes. The electron–current increment dI_n has the same magnitude as dI_p, but is negative in this convention,

$$dI_n = -(\alpha_p\,I_p\,dx + \alpha_n\,I_n\,dx). \tag{3-7}$$

Because $I = I_p + I_n$ in the depletion region, $(I - I_p)$ can be substituted for I_n in Eq. (3-6) yielding

$$\frac{dI_p}{dx} - (\alpha_p - \alpha_n)\,I_p = \alpha_n\,I. \tag{3-8}$$

This is a first–order nonhomogeneous differential equation with general solution

$$I_p(x) = \frac{\int_0^x \alpha_n\, I\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx' + C}{exp\left[\int_0^x -(\alpha_p - \alpha_n)\, dx'\right]} \qquad (3-9)$$

where C is a constant of integration. For the initial condition, $x = 0$, C is equal to $I_p(0)$. When $x = W$, Eq. (3-9) becomes

$$I_p(W) = \frac{\int_0^W \alpha_n\, I_p(W)\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx' + I_p(0)}{exp\left[\int_0^W -(\alpha_p - \alpha_n)\, dx'\right]} \qquad (3-10)$$

where I has been replaced by $I_p(W)$ because there is only an extremely small leakage current at this boundary. A new factor, M_p, is now introduced and is defined as:

$$M_p \equiv \frac{I_p(W)}{I_p(0)}. \qquad (3-11)$$

This term, M_p, is known as the multiplication factor for holes and is equal to the ratio of hole currents at the boundaries.

If both sides of Eq. (3-10) are divided by $I_p(W)$ and the hole multiplication factor is introduced, the following equation results:

$$\frac{1}{M_p} = exp\left[\int_0^W -(\alpha_p - \alpha_n)\, dx'\right] - \int_0^W \alpha_n\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx'. \quad (3-12)$$

A simpler form of this equation can be found by a somewhat tedious manipulation. First, add and subtract the term

$$\int_0^W \alpha_p\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx' \qquad (3-13)$$

to and from the right–hand side of Eq. (3-12). Grouping this positive added term with the last term of Eq. (3-12) yields the expression,

$$-\int_0^W -(\alpha_p - \alpha_n)\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx' \qquad (3-14)$$

which is equal to:

$$-\int_0^W \frac{d}{dx'}\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx'$$

$$= -exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right]_0^W$$

$$= -exp\left[\int_0^{W} -(\alpha_p - \alpha_n)\, dx''\right] + 1. \qquad (3-15)$$

This term is now substituted back into Eq. (3-12) canceling the first term in Eq. (3-12) leaving 1 and the negative added term of Eq. (3-13):

$$\frac{1}{M_p} = 1 - \int_0^W \alpha_p\, exp\left[\int_0^{x'} -(\alpha_p - \alpha_n)\, dx''\right] dx', \qquad (3-16)$$

or

$$1 - \frac{1}{M_p} = \int_0^W \alpha_p\, exp\left[\int_0^{x'} (\alpha_n - \alpha_p)\, dx''\right] dx'. \qquad (3-17)$$

The resulting multiplication factor is used for the determination of avalanche breakdown for an np^+ junction. Similarly, the equation for determining the avalanche breakdown in a pn^+ junction is

$$1 - \frac{1}{M_n} = \int_0^W \alpha_n\, exp\left[-\int_{x'}^{W} (\alpha_n - \alpha_p)\, dx''\right] dx'. \qquad (3-18)$$

It has been demonstrated that the reverse current of an np^+ diode approaches infinity at a more rapid rate than a pn^+ diode [25]. The expression on the right–hand side of Eq. (3-17) or Eq. (3-18) is known as the *ionization integral.* Using the approximation for the ionization coefficients in Eq. (3-3), the ionization integral reduces to

$$1 - \frac{1}{M_x} = \int_0^W \alpha_{eff} \, dx \qquad (3-19)$$

As the reverse–bias voltage on a junction is increased, the electric field in the depletion region increases, too. This causes α_n and α_p to rise steeply, as could be seen in Fig. (3-1). As a consequence, M_p increases in the same proportion, and small increments of reverse–bias voltage produce large increments of "avalanche" current. Breakdown is defined to occur when $M_p \longrightarrow \infty$, but for computer simulations in this work, breakdown was assumed to occur when M_p reached the value of 10 [29].

The breakdown condition of devices is analyzed by the computer code used in this work, using numerical integration techniques described in the next chapter. The calculations are performed by selecting paths through points in the device structure containing the highest electric fields. This approach has been found to be effective in accurately predicting the avalanche breakdown of junctions for a large variety of terminations while avoiding the complexity of analyzing all possible avalanche multiplication paths [11]. The computer code determines the ionization path by starting from the peak electric field location and following the potential gradient line in both directions [2].

3.2 One–Dimensional Abrupt Junction Diode

The analysis of the potential and electric field distributions in semiconductor devices will be considered in a simple one–dimensional abrupt *p-n* junction

shown in Fig. (3-3). In this diode, the doping concentration on the p^+ side of the junction is much greater than the lightly doped n^- side. Devices fabricated with shallow junctions can be represented by this shallow junction case, especially when the doping level of the substrate is low. In these cases, the depletion layer extends primarily into the lightly doped side.

For the case of this np^+ junction, with a reverse–bias voltage V_D applied, Poisson's equation needs to be solved only for the n side. This is due to the fact that the depletion layer extends almost entirely into the n side as a result of the very high doping level on the p^+ side. The one-dimensional Poisson equation can be expressed as

$$\frac{d^2V}{dx^2} = \frac{-dE}{dx} = \frac{-Q(x)}{\epsilon_s} = \frac{q\,N_D}{\epsilon_s} \qquad (3-20)$$

where $Q(x)$ is the charge in the depletion region due to ionized donors, ϵ_s is the dielectric constant of the semiconductor, q is the electronic charge, and N_D is the donor doping density.

The electric field distibution is obtained by integrating Eq. (3-20):

$$E(x) = \frac{q\,N_D}{\epsilon_s}\Big(W - x\Big) - E(W). \qquad (3-21)$$

The assumption is made that the junction is deep enough so that $E(W) = 0$. The electric field varies linearly with distance as shown in Fig. (3-3). The potential (voltage) distribution is then obtained by integrating Eq. (3-21) knowing that $E(W) = 0$, $V(W) = V_D$, and $V(0) = 0$:

$$V(x) = \frac{q\,N_D}{\epsilon_s}\Big(Wx - \frac{x^2}{2}\Big). \qquad (3-22)$$

The potential varies quadratically with distance as illustrated in Fig. (3-3). It can be shown that the depletion layer width can then be calculated with the boundary

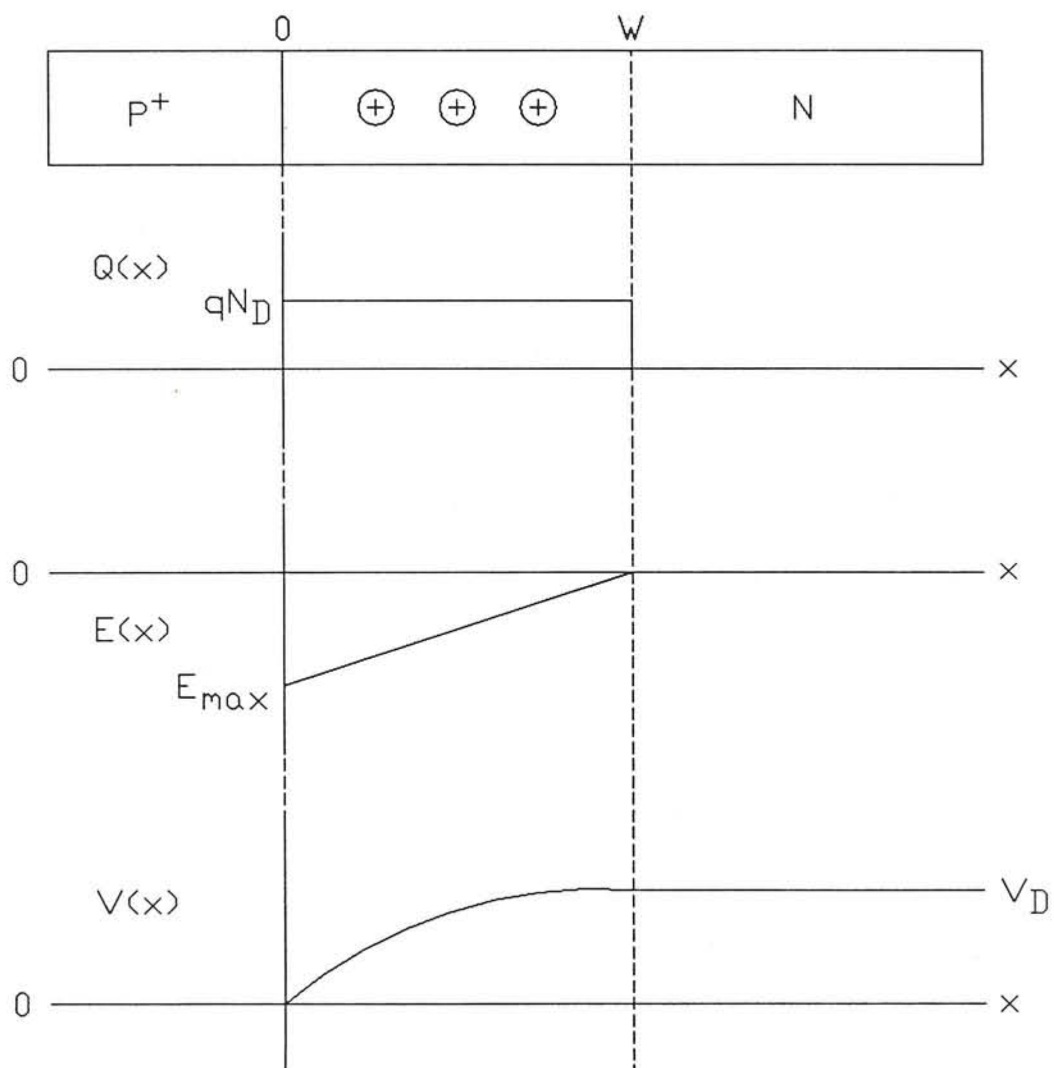


Figure 3-3. Potential and electric field distributions in an abrupt reverse–biased *p-n* junction. (After Baliga [11].)

condition that the potential at $x = W$ must equal the applied reverse–bias voltage, V_D:

$$W = \sqrt{\frac{2\,\epsilon_s\,V_D}{q\,N_D}}. \qquad (3-23)$$

From Eq. (3-23), the maximum electric field occurs at $x = 0$. Substituting Eq. (3-23) in Eq. (3-21) yields an equation relating the maximum electric field to doping concentration (N_D) and applied reverse–bias voltage (V_D):

$$E_{max} = \sqrt{\frac{2\,q\,N_D\,V_D}{\epsilon_s}}. \qquad (3-24)$$

The electric field expressions can be combined with equations (3-3) and (3-19) to derive a closed–form analytical expression for the depletion layer width at breakdown. From the breakdown conditions and the field dependence of the ionization rates described in the previous section and the maximum electric field equation (Eq. (3-24)), the breakdown voltage can be described as [52]

$$V_{BD} = \frac{\epsilon\,E_{max}^2}{2\,q\,N_{BC}}. \qquad (3-25)$$

Fig. (3-4) shows this calculated breakdown voltage versus the background doping concentration (N_{BC}) for abrupt junctions in Si, Ge, GaAs, and GaP [50]. The dashed line represents the limit of N_{BC} for which the avalanche breakdown calculation (Eq. (3-25)) is valid. The calculated values are in good agreement with experimental results [60].

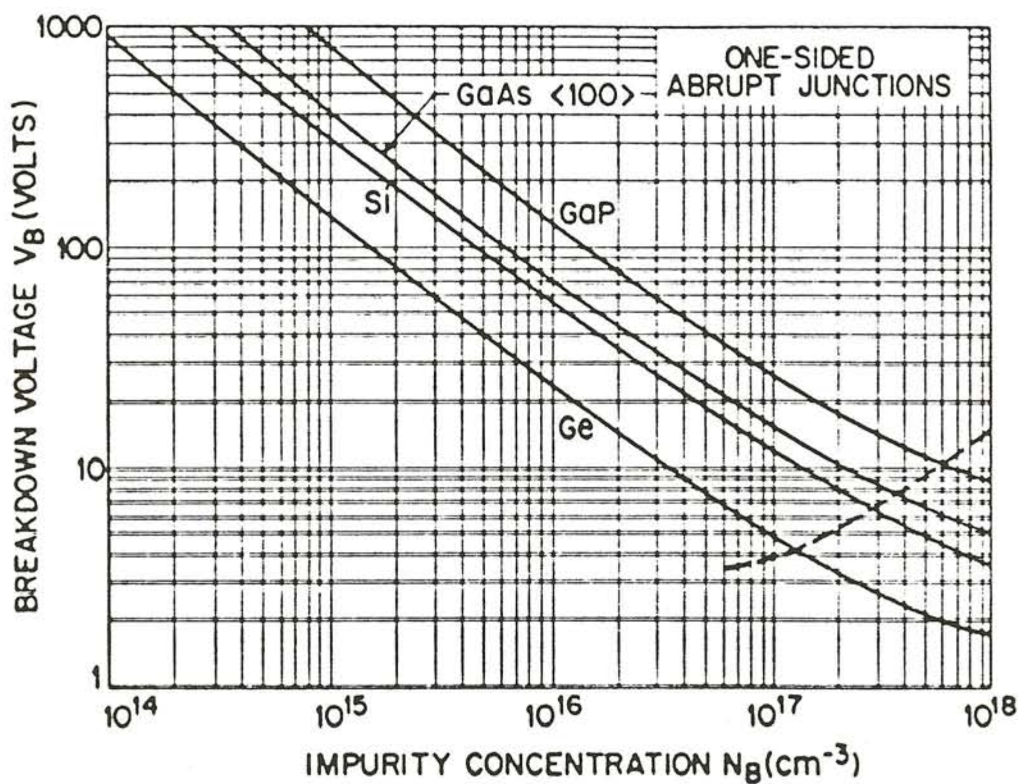


Figure 3-4. Breakdown voltage versus substrate impurity concentration for one-sided abrupt junctions in Si, Ge, GaAs, and GaP. (After Sze and Gibbons [50].)

CHAPTER 4
METHOD OF SIMULATION

To aid in the investigation of power semiconductor devices under the highly reverse–biased condition, a two–dimensional simulation program has been developed. The code, which has been given the name SEPSIP (SEmiconductor Power device SImulation Program), assumes the device is in a static equilibrium state. Wu [65] wrote the original device simulation program entitled HVDS (High–Voltage Device Simulator) which used Gaussian elimination to solve the system of equations. Yen [68] revised this code by employing the Newton successive overrelaxation method to solve the nonlinear difference equations for the potential distributions of arbitrary sections of semiconductor devices, and gave the new code the name SEPSIP. This code has since been modified and enhanced through this work and the work of Tan [53] to incorporate the ability to simulate a wider variety of device structures (Version 2.0). Yen [68] has described the numerical methods used in the code, and a current set of instructions for executing the program have been described by Tan [53]. In this chapter, a brief overview of the SEPSIP code will be presented.

Electrical behavior in a semiconductor device is described by Poisson's equation and the current continuity equations. Unlike in Section 3.2 where a one–dimensional representation of Poisson's equation was presented, solving Poisson's equation now has been expanded to two dimensions. Discretization of the solution domain and the setting up of the difference equations will be discussed. Changes

made to the code, relating to these topics, in order to simulate more complex structures will be given.

4.1 Poisson's Equation

Poisson's equation is a continuity equation that expresses the continuity of lines of force. A fictional line originates from a positive charge and terminates on a negative charge of the same magnitude. The magnitude of these charges is chosen randomly, but often it is convenient to use q, the elementary electronic charge, for this purpose. So, a line of force begins at a $+q$ charge and ends at a $-q$ charge, and the direction of this line is the direction of the electric–field vector, E. The density of these lines at any one point will be proportional to the electric–field strength which has units of V/cm. The electric–field vector quantity exhibits a positive divergence in a volume having a net positive charge, and a negative divergence in a volume having a net negative charge.

Electrical behavior, namely the potential distribution, in a semiconductor device is determined by solving the Poisson equation and the current continuity equations. For power devices subject to high reverse–bias voltages, it can be assumed that zero current density exists [52]. Under this assumption, carrier and potential distributions can be obtained accurately from Poisson's equation alone. Poisson's equation can be written in a fairly general form as:

$$\nabla^2\psi = \frac{-\rho}{\epsilon} \qquad (4-1)$$

where the resistivity or total charge density is given by

$$\rho = \begin{cases} q\,(N_D - N_A + p - n) & \text{for semiconductor material;} \\ 0 & \text{for most dielectric material,} \end{cases} \qquad (4-2)$$

and ϵ, the absolute permittivity, is the product of the permittivity of free space,

$$\epsilon_o = 8.85 \times 10^{-14}\, F/cm, \qquad (4-3)$$

and ϵ_r, the relative dielectric permittivity or dielectric constant of the sample. For silicon, ϵ_r has been determined to range from about 11.4 to 12.0. In this work, a value of 11.9 has been chosen to represent this constant. In Eq. (4-2), N_D and N_A denote the densities of ionized donors and acceptors, respectively, and by using Boltzmann's approximation, the carrier concentrations can be expressed as

$$\begin{aligned} n &= n_i e^{\frac{q}{kT}(\phi-\phi_n)} \\ p &= n_i e^{\frac{q}{kT}(\phi_p-\phi)} \end{aligned} \qquad (4-4)$$

where n_i is the intrinsic carrier concentration and the quantity $\frac{kT}{q}$ is often referred to as the thermal voltage. ϕ_p and ϕ_n are the quasi-Fermi levels and are constant for a reverse–biased junction.

For any three–dimensional volume, V, the integral form of Poisson's equation is obtained as

$$\int_V -\nabla \cdot (\epsilon \nabla \psi)\, dv = \int_V \rho dv \qquad (4-5)$$

provided that the potential, ψ, is continuous and $\epsilon\nabla\psi$ has a finite number of discontinuities in the region of interest. The left hand side of (4-5) can be converted into a surface integral by the divergence theorem. Taking discontinuities of charged surface (A') into account, Eq. (4-5) is equivalent to

$$\oint -\epsilon \frac{\partial \psi}{\partial m} da = \int_V \rho dv + \int_{A'} \rho_{ss} da'. \qquad (4-6)$$

This form is known as Gauss' Law of electromagnetics. It states that the electric field flux, $-\epsilon\frac{\partial\psi}{\partial m}$, flowing out of a surface is equal to the charge enclosed. Because

two-dimensional analysis describes the area of interest with great accuracy, it is desired to reduce Eq. (4-6) by one dimension,

$$\oint -\epsilon \frac{\partial \psi}{\partial m} ds = q_v + q_{ss} \tag{4-7}$$

where

$$\begin{aligned} q_v &= \int_A \rho da, \\ q_{ss} &= \int_L \rho_{ss} dl. \end{aligned} \tag{4-8}$$

This leaves equation (4-7) that can be solved quite readily by computer. Iterations involve updating the potential and carrier concentrations until a certain accuracy is achieved [68]. Simulation times required to converge to a solution are dependent on the number of nodes in the grid distribution, the biasing voltage and the type of computer used.

4.2 Overview of the SEPSIP Code

There are several input parameters to the SEPSIP code. Detailed explanations of these parameters for the most recent version of the code are given by Tan [53]. The parameters that this work is most concerned with are those describing how to discretize the solution domain and the surface–charge density present at the silicon–silicon dioxide interface during simulation. A brief discussion of these small portions of SEPSIP will be given in the next few sections.

4.2.1 Grid Spacing Between Nodes

Because the power device structures to be simulated were much wider in size than the capabilities of the original version of the code allowed, changes needed to be made in the discretization scheme. Also, very thin oxide layers in the range

of hundreds and thousands of Å, and floating field rings were present in the power device structures that were thought to be insensitive to varying surface charges. It was desired to place a denser pattern of nodes in the areas around and between field rings so that a more accurate solution could be obtained in these areas. To incorporate the ability to describe the structures with greater numbers of nodes, the dimensions of several variables had to be increased from 100 to 200. To simulate the wider structures and to obtain valid results for the electric field, the variable *scale* had to perform properly. This variable describes the number of microns per drawing unit and it is very important in determining the electric field intensities at all the nodes.

In the x or y direction of the structure, a transition from a dense area of nodes to an area of less interest had to be made gradually. The code does not allow two adjacent spacings to differ by more than 25%. This feature exists so that numerical errors will be kept to a minimal. A minimum of three nodes are placed in any region no matter how small. An example of this is the thin oxide layers where three nodes are placed in this layer (y direction) and the initial spacing of nodes above and below the oxide layer is the same as that inside the oxide layer. Outside the oxide layer, the spacing of nodes gradually increases, though, but not by more than 25%. From the output file, the user of the code is given all node spacings and can determine if they are to his liking.

4.2.2 Surface–Charge Density

Surface–charge density is one of the most important SEPSIP parameters used in this work. It was desired to examine device behavior over a range of surface charges for a number of structures. This was accomplished by changing this parameter before each run of the simulation. With increased surface charge, it can be

assumed that the breakdown voltage will decrease. Accordingly, the biasing voltage was adjusted before each run.

As was mentioned earlier in Section 2.3, N_{ss} represents the algebraic difference between the positive oxide trapped charge and the negative interface trapped charge and is taken as positive in this work. In Eq. (4-7), it was shown how this trapped charge influences the potential. SEPSIP draws a rectangular box around each node of the discretized domain of the structure being simulated, and computes the charge enclosed. The magnitude of N_{ss} is added to this charge only for those nodes at the surface.

4.3 Ionization Integral

It was discussed in Section 3.1.2 what physically takes place when a *p-n* junction breaks down. The enhancement of computing the breakdown condition has been added to the SEPSIP code. This involves computing the ionization integral along the ionization path through the peak electric field. After computing the electric–field distribution, SEPSIP finds the node with the maximum electric field. From this point, the potential gradient in both directions is found [2]. The next node along the potential gradient is the one with the smallest electric–field value. This process is continued in both directions until a small electric–field magnitude is found. The ionization rates (α_p and α_n) will be negligible at the ends of the ionization path because of their dependence on the electric field. Avalanche multiplication calculations can be made along all possible avalanche paths, but the most likely path to have the largest ionization integral value is the path through the peak electric field [11].

Eq. (3-17), the ionization integral for holes, shall be repeated here for reference:

$$1 - \frac{1}{M_p} = \underbrace{\int_0^W \underbrace{\alpha_p \, exp \underbrace{\left[\int_0^{x'} (\alpha_n - \alpha_p) \, dx'' \right]}_{f(n)}}_{g(n)} dx'}_{h(n)}. \qquad (4-9)$$

Solving this integral equation by breaking it up into discrete increments will be discussed, but not in great detail. Both α_p and α_n are dependent on the electric field. These are calculated first using the expressions given by Sze and Gibbons [50] at each node along the ionization path. Both integrals of Eq. (4-9) are then calculated in the same step for a change in distance between two nodes: The inner integral from 0 to x' includes all increments from the beginning of the path to the present increment of the path. The outer integral from 0 to W describes the path through the whole depletion layer. This means that the previously computed values of the inner integral are summed together before the outer integral is computed for each increment of the path. All computed values of the outer integral are summed together to give an expression for the right–hand side of the equation. This value can never be greater than 1 and breakdown is assumed to occur when it approaches 1 ($M_p \longrightarrow \infty$) as was discussed in Section 3.1.2. Experimenting with an M_p value that would describe breakdown well, and comparing results with those made by Hwang and Navon [29], it was determined that an M_p of 10 gave good values of breakdown voltage for a number of structures being simulated. Due to the dense pattern of nodes surrounding a junction, the Δx increment in the ionization path will be small resulting in a more accurate solution of the ionization integral.

4.4 SEPSIP Output

In addition to the *file*.OUT output file being created by SEPSIP, *file*.PTH is created if the *breakv* input parameter is set true. In this file, the nodes along the ionization path are given as well as their physical x and y locations. The electric–field magnitude and the ionization rates (α_p and α_n) are presented for each node. The inner integral calculated for each increment is given as $f(n)$ where n is the number of the increment. For example, $f(12)$ would contain the value of f from the 11th to the 12th node of the path plus $f(11)$. $g(n)$ is the product of $\alpha_p(n)$ and $exp(f(n))$. $h(n)$ is then the integral of $g(n)$, plus $h(n-1)$ added to it.

Likewise, these same f, g, and h variables are used for the pn^+ ionization integral of Eq. (3-18). This integral equation is computed from W to 0 because of the bounds of the inner integral. These computed values are presented in the *file*.PTH file in a similar manner. At the end of the file, M_p and M_n are given. The user of the code obviously knows which type of junction exists in his structure and can determine which multiplication factor to consider. If both types of junctions exist in the structure, then the location of the ionization path can be used to determine which junction broke down.

In a future version of SEPSIP, the ionization path may be drawn on the AutoCAD output drawing. This feature can easily be added in the code by making use of the existing subroutine WRDXF (and perhaps a *ploti* input parameter). However, the peak electric field is drawn on this drawing as well as the potential distribution. Therefore, one can visualize the ionization path through the peak electric field and orthogonal to equipotential lines.

CHAPTER 5

HIGH-VOLTAGE JUNCTION TERMINATION TECHNIQUES

The abrupt junction described in Section 3.2 was assumed to be one-dimensional and semi-infinite. Edge effects were not considered in deriving the equations that describe the junction. For practical devices, it becomes necessary to include these edge effects. Actually, the edge termination limits the breakdown voltage of practical devices to a value below the theoretical breakdown voltage obtained from the semi-infinite junction.

With the introduction of planar diffusion technology, it became possible to fabricate a large number of devices on a single wafer by carefully diffusing impurities through a silicon-dioxide masking layer. The drawback of this process is that it creates cylindrical junctions at the mask edges and spherical junctions at the sharp corners of the diffusion window. Junction curvature cannot be neglected in the design of high-voltage devices.

Due to the curvature of the planar junction and its effect on the breakdown voltage, methods to reduce the depletion layer curvature have been investigated. These methods include the use of floating field rings and equipotential field plates. Recently, ion implantation has become a useful means of controlling the charge at the surface for improving the electric field distribution and increasing the breakdown voltage. This technique is known as junction termination extension [10].

In this chapter, planar-junction theory is discussed. Theoretical background for improving this type of junction with field rings and field plates is given.

These techniques are then compared based on the application for various types of power devices.

5.1 Planar Diffused Terminations

The most widely used termination for low current devices where many devices are fabricated on each wafer is the planar–diffused termination [11]. This type of junction involves selectively introducing dopants into the semiconductor surface through the oxide masking layer. In addition to the dopant diffusing down into the semiconductor, also it diffuses laterally at the edges of the diffusion window as shown in Fig. (5-1). This lateral diffusion has been analyzed to extend to about 80% of the junction depth [43]. The depletion layer of the junction follows the cylindrical and spherical contours of the junction. Also, the potential follows these contours, but the electric field, which points orthogonally to the equipotential lines, crowds in these curved portions of the junction because charge between the two sides of the junction must be balanced as shown in Fig. (5-2). In the case of the np^+ junction, the electric field lines would be in the opposite direction. The higher electric field at the curved portions of the junction leads to a larger impact ionization at the edges. Consequently, breakdown of the junction is expected to occur at the curved portion rather than in the parallel–plane portion.

The junction curvature of the abrupt planar junction significantly reduces the breakdown voltage from the "ideal" one–dimensional structure. Sze and Gibbons [50] have compared ideal breakdown voltages with the curvature effects [51]. These results are presented in Fig. (5-3) where an abrupt silicon junction's breakdown voltage is plotted versus substrate impurity concentration. It is shown that the more shallow junction depths have remarkedly lower breakdown voltages due to the increased crowding of the electric field which was shown in Fig. (5-2).

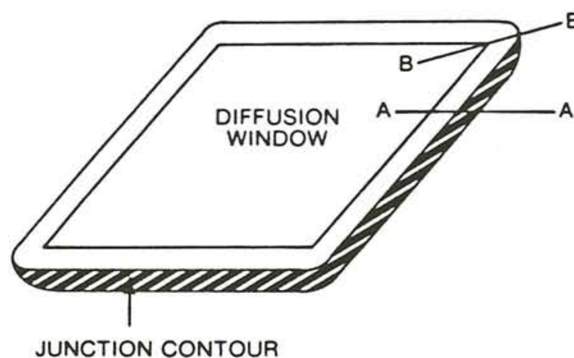


Figure 5-1. Planar junction formed by diffusion through a rectangular diffusion masking window. (After Baliga [11].)

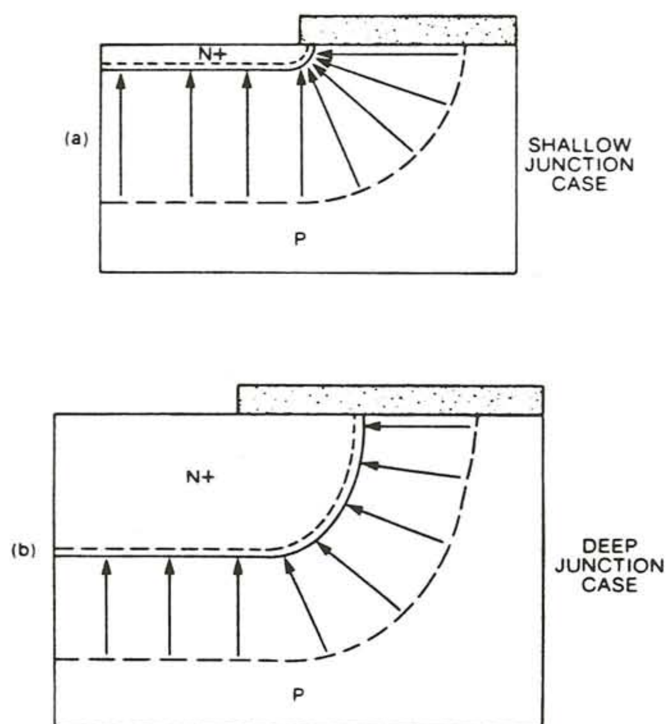


Figure 5-2. Electric field distribution and crowding at the edges of a (a) shallow and a (b) deep junction. (After Baliga [11].)

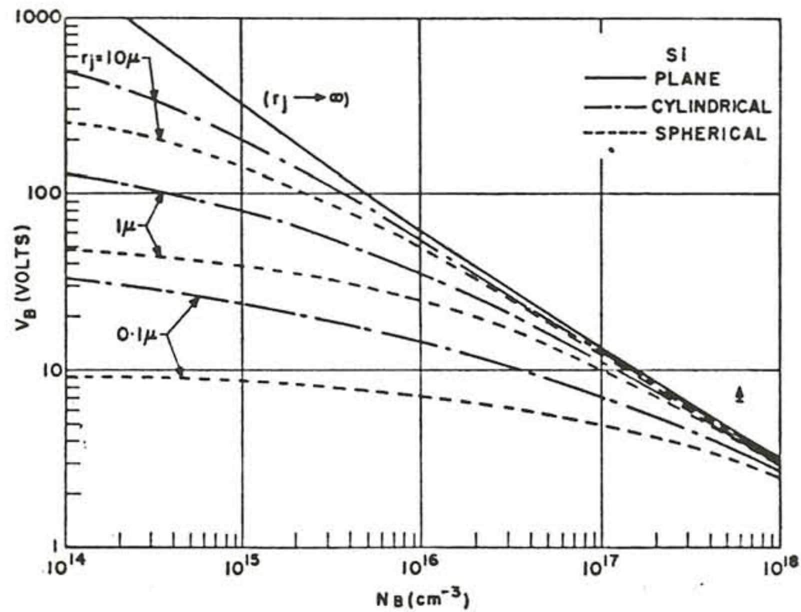


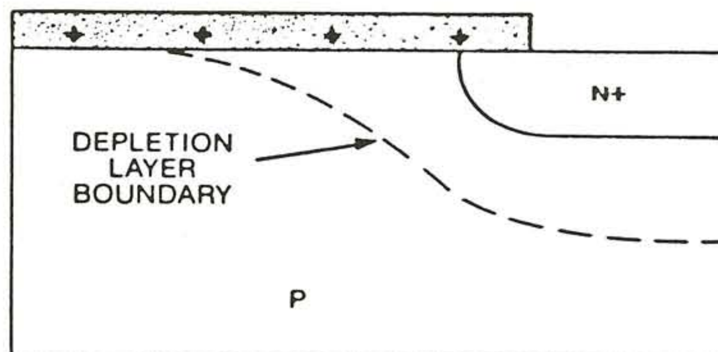
Figure 5-3. Breakdown voltage, V_B, versus substrate impurity concentration, N_B, for different junction radii, r_j, for abrupt junctions in Si. (After Sze and Gibbons [51].)

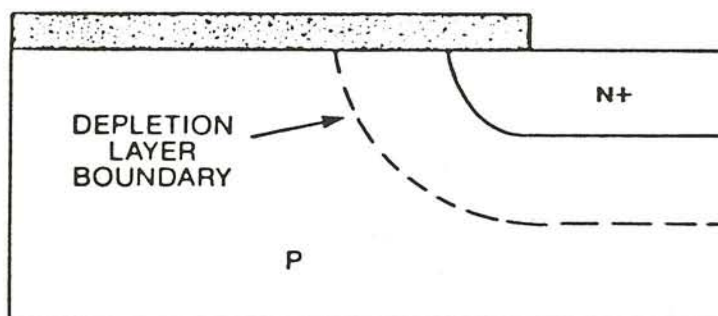
Fig. (5-4) shows the influence of surface charge on the depletion layer of a planar junction. The depletion layer spreading is greatly affected at the surface because this charge complements the charge due to ionized acceptors inside the depletion layer. Positive surface charge results in a spreading of the depletion layer at the surface in a pn^+ junction and causes shrinking in an np^+ junction. Negative surface charge causes opposite effects in these two types of junctions.

5.2 Floating Field Rings

It has been known for some time that by the use of one or more floating field rings reduces the effects of junction curvature [30]. These effects are electric field crowding in the curved regions of the junction and increases in the electric field at the surface. As shown in Fig. (5-5), a concentric ring junction surrounding the main junction can be diffused by the same process as the main junction. When they are fabricated simultaneously, their diffusion depths will be equal. The spacing of this ring is such that, at a voltage much lower than the breakdown of the bulk or the flat portion of the junction, the depletion or space–charge region of the main reverse-biased junction will punch–through to the ring well before the critical electric field for breakdown is attained. A cross-section along C-C in Fig. (5-5) is shown in Fig. (5-6) with the depletion region boundaries shown. It can be seen that the electric field crowding present in the curved areas of a planar junction without a field ring is reduced by the addition of the floating ring. This is the same crowding responsible for low breakdown voltages of the junction.

After punch-through to the ring, any increase in voltage will be taken up by the ring junction as the carriers are depleted on the outside of the ring as is shown in Fig. (5-6). In this figure, it was assumed that no surface charge existed at the silicon–silicon dioxide interface and punch–through occurred at the surface.





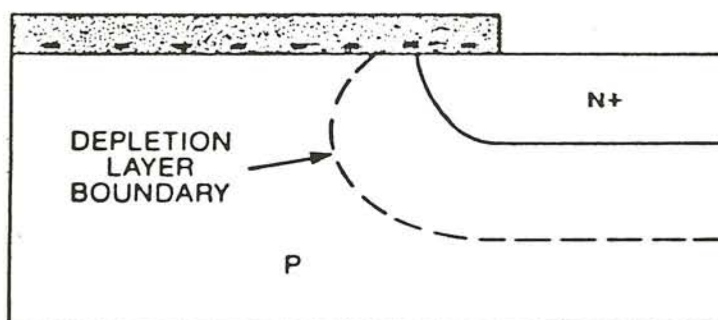


Figure 5-4. Surface charge influence on the depletion layer at the edge of a planar junction: (a) positive charge; (b) zero charge; (c) negative charge. (After Baliga [11].)

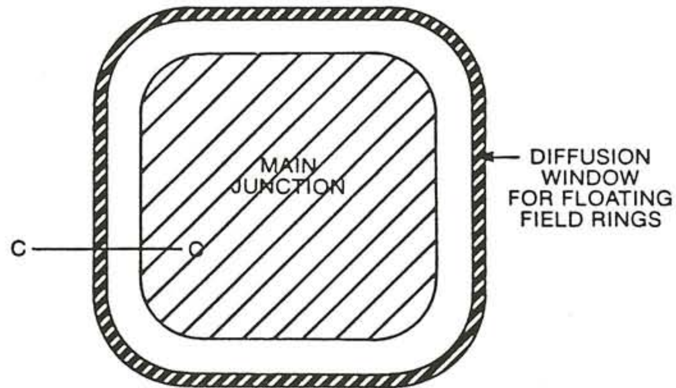


Figure 5-5. Diffusion window with one floating field ring. (After Baliga [11].)

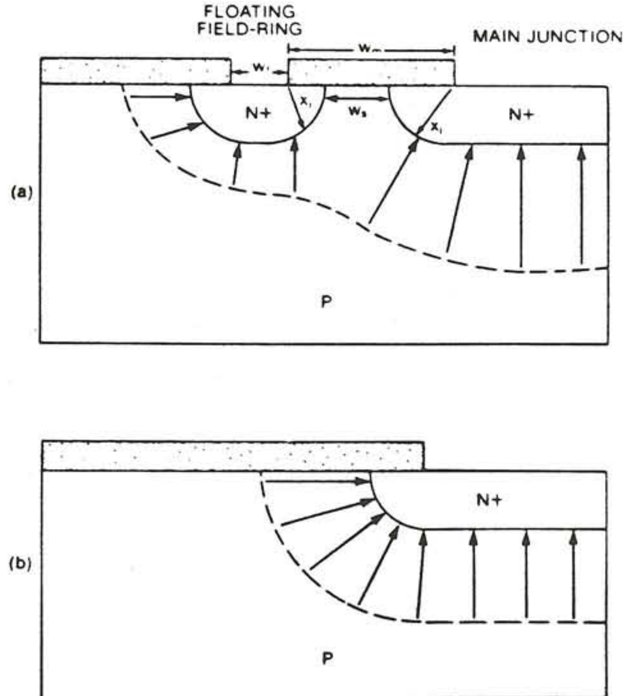


Figure 5-6. Comparison of the electric field crowding for a planar junction (a) with and (b) without a floating field ring. (After Baliga [11].)

Intuitively, the floating field ring is expected to reduce the electric field crowding, but its spacing from the main junction is crucial in determining its effectiveness in increasing the breakdown voltage. If it is placed too far from the main junction, then breakdown will occur on the main junction rendering the field ring ineffective. If it is too close, its potential will nearly be the same as the main junction and it will have the same curvature as the main junction increasing breakdown voltage only slightly. However, optimally placing the field ring can result in a doubling of the breakdown voltage [2]. This optimal spacing depends on the oxide thickness and doping concentration. Optimality is achieved when avalanche multiplication occurs at the outer edges of the ring and main junction simultaneously [16]. At this point, it should be at least qualitatively clear why field rings help reduce the effect of junction curvature since the constant potential lines no longer follow the curvature of the main junction.

Changes in surface charge can increase or decrease breakdown voltage depending on the doping, but it is most likely that the latter will happen, especially with large amounts of surface charge. When a fixed surface charge is precisely known, it is possible to analyze the optimal location of the field ring, but when the surface charge is varied, limitations exist in designing the breakdown of floating field ring devices. The use of a one–dimensional model to determine the punch–through voltage to the ring is valid when no surface charge exists. However, some surface charge almost always exists, and punch–through occurs below the surface [2]. Fig. (5-7) shows this event taking place where positive charges are assumed in the oxide shrinking the depletion layer at the surface. It is interesting to note that beyond punch-through there is predicted to be a triangular pocket of undepleted semiconductor at the surface next to the ring on the main junction side.

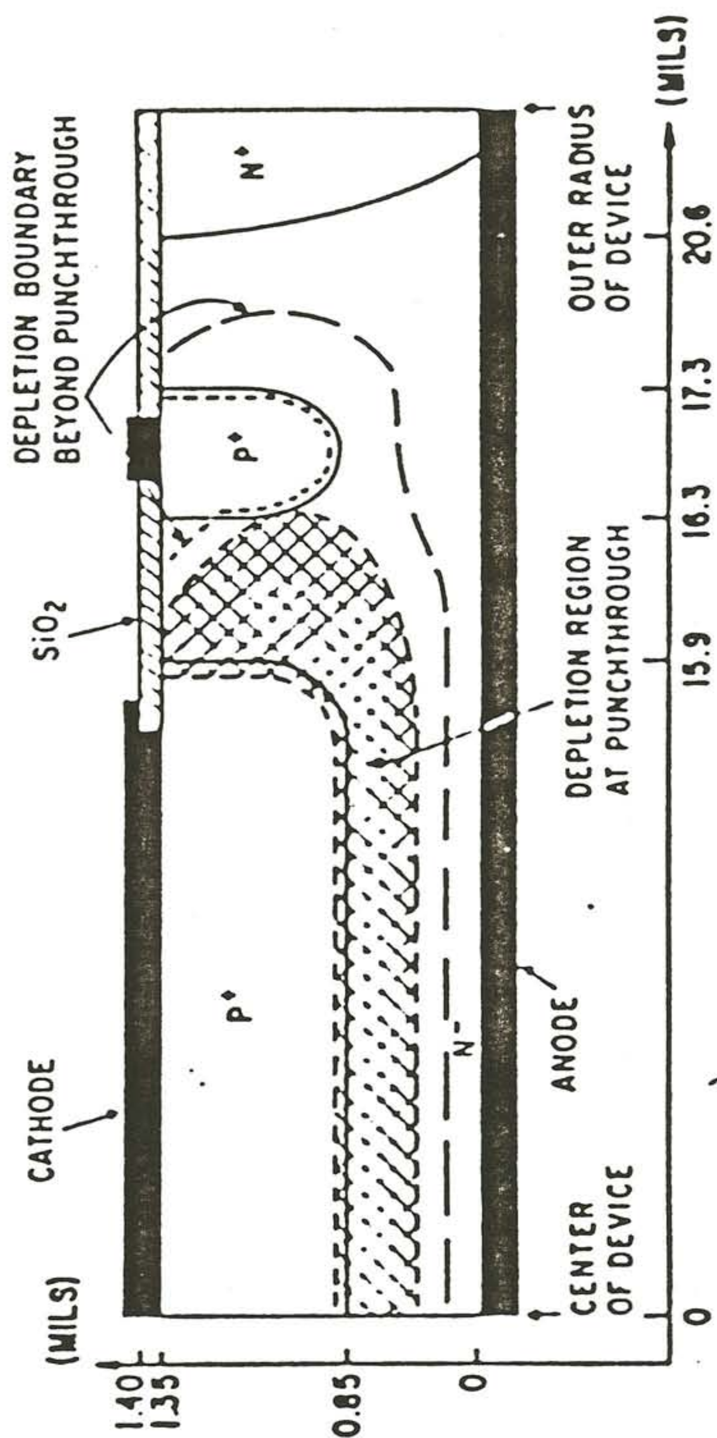


Figure 5-7. Surface charge effects of the depletion layer punching-through to the floating field ring. (After Adler, *et al* [2].)

Either positive or negative surface charge during fabrication almost variantly exists in the oxide of semiconductor devices. In practice, the number of positive surface states of thermally oxidized silicon ranges from 10^{10} to $10^{12}\,cm^{-2}$. Even with a well–controlled, clean fabrication sequence, the surface state density will vary from wafer to wafer and even across a single wafer by $\pm 1 \times 10^{11}\,cm^{-2}$. This variation places a practical limitation on the design of an optimal structure with one floating field ring.

The effectiveness of the floating field ring is the greatest for high–voltage devices fabricated with shallow junctions [11]. For deep junctions, the curvature effects are small to begin with. The addition of a field ring will raise the breakdown voltage by only a smaller amount and take up much valuable space on the chip. It is more common to use field rings in power devices operating at voltages lower than $1500\,V$. Equally important to ring depth is the width of the ring. Even if the ring is optimally located, a narrow ring can be ineffective in reducing the depletion layer curvature. A ring that is too wide is not advisable because it does not improve the breakdown voltage. Instead, it wastes space at the edge of the chip. The width of the ring should be comparable to the depletion layer width. This field ring width should be in the neighborhood of three times the ring depth [16].

5.3 Multiple Floating Field Rings

If one ring can raise the breakdown voltage by a factor of nearly two, then it can be expected that several floating field rings working in conjunction with one another can raise the breakdown voltage so as to approach the parallel-plane case. It is as easy to fabricate several rings as it is to fabricate just one ring because the rings are diffused at the same time as the main junction by designing the mask with multiple windows surrounding the main junction. But, the area on the chip

then increases. Again, the spacing, depth, and width of the rings must be designed intelligently.

There exist a few different philosophies for the design of multiple floating field ring terminations. In one, both the spacing and the width of the rings should decrease as distance from the main junction increases. Because the depletion layer widths below the field rings further away from the main junction are smaller, these rings can be made narrower. Also, this saves space at the device perimeter. There is one major drawback to this approach, though. The surface charge must be precisely known and stable for this structure to effectively increase the breakdown voltage. Small changes in surface charge have a big effect in making the inner rings useless.

In another approach, all the floating rings are equally spaced and made narrow. More rings can be fabricated in a given area with this method. The lower edge of the depletion region is steeper as it approaches the surface in this design. The spacing is not optimal because breakdown will not take place on all rings concurrently. The larger number of rings and smaller spacing between them makes this structure less sensitive to surface charge, but it is not the least sensitive.

Several researchers [15,16,30] and this work, have found that optimal spacing between rings progressively increases as distance from the main junction increases as shown in Fig. (5-8). The width of each ring is the same and approximately equal to three times the junction depth as was mentioned in the previous section. With increased number of rings in the structure, the spacing between the rings would be smaller. Variations in surface charge have less of an effect on the transferring of potential between rings because the substrate between rings at higher potentials is very narrow (experimental data is shown in Fig. (6-14)). It is true, though, that at greater surface charges, punch–through to the last ring or rings will not happen. In all of these multiple floating field ring design approaches, the intent

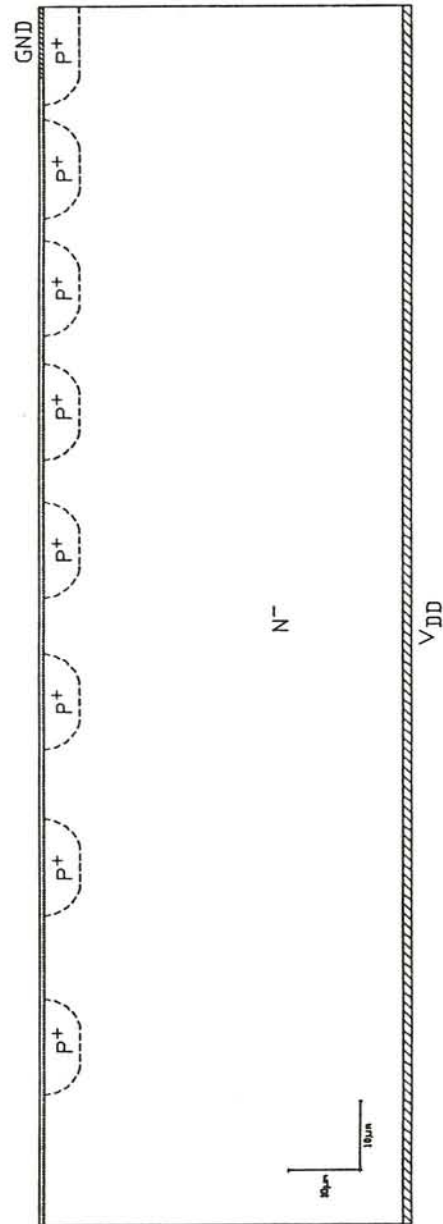


Figure 5-8. Cross-section of a seven-ring termination structure.

is to spread out the depletion layer at the surface over a great distance allowing the structure to resemble a parallel–plane junction.

5.4 Equipotential Field Plates

In previous sections, it was discussed that junction curvature causes the high electric fields that lead to unfavorable breakdown voltages. To help spread out the depletion region at the surface, the surface potential needs to be controlled. The simplest method to alter the surface potential is the addition of a metal field plate over the oxide at the edge of the planar junction as shown in Fig. (5-9). The depletion layer shape then can be adjusted by changing the bias of the field plate in the same way surface charge does as was shown in Fig. (5-4). When a positive bias is applied to the plate, electrons will be attracted to the surface of the n-type substrate causing the depletion layer to shrink (case A). A negative bias will have the effect of expanding the layer (case C). This expansion will reduce the junction curvature and increase the breakdown voltage [27]. Opposite biasing effects will occur for a pn^+ junction.

Because the favorable biasing polarity is the same as the main junction's polarity, and because it is impractical to provide a separate bias on the field plate, field plates are created merely by extending the junction metallization over the oxide as shown in Fig. (5-10). A field plate alters the surface potential by acting through the oxide layer to force the depletion layer to extend at the surface beyond the edge of the field plate. This "stretching out" of the depletion region reduces the depletion layer curvature and, in turn, reduces the peak electric field. However, a high electric field can occur at the edge of the field plate at point A if the oxide layer is too thin or the field plate extends too far [19]. The optimum oxide thickness and field plate length are achieved when the peak electric fields at points A and B

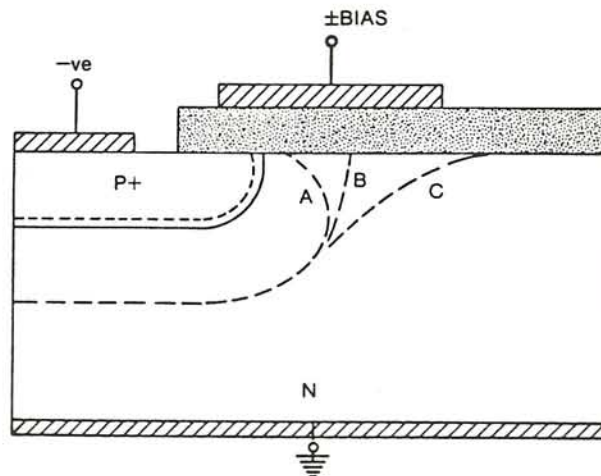


Figure 5-9. Planar junction with an externally–biased field plate at the edge of the junction. (After Baliga [11].)

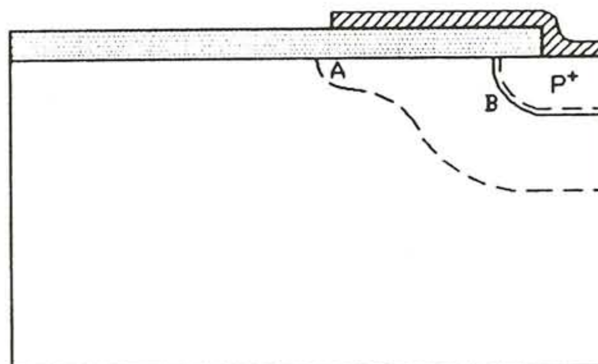


Figure 5-10. Field plate termination structure formed by extending the metallization over the oxide at the junction edge. (After Baliga [11].)

are equalized [11]. Instead of balancing the fields at these two points, a method of varying the oxide thickness from small values near the junction to thicker values at the edge of the field plate has been experimented with. This method requires a complex device fabrication process that is not justified by the increase in breakdown voltage.

Calculation of the ionization integral at the edge of the field plate indicates that to avoid breakdown here the depletion layer width (x_d) to oxide thickness (x_o) ratio (x_d/x_o) should be less than 12 [19]. This implies that in order to spread out the depletion region to reduce the junction curvature, a sufficiently large oxide layer will need to accompany a long field plate. However, if the oxide is too thick, the influence of the field plate on the junction curvature diminishes, and breakdown most likely will occur at the metallurgical junction.

Thicker oxide layers invite unwanted surface charges, though. A field plate functions by modifying the charge in the oxide. When ionizing radiation is altering the charge at the same time, undesired results may occur. In Fig. (5-11), a field plate device and surface charge variation results are presented [19]. This structure not only has a field plate over the main np^+ junction, the substrate is connected to one that extends over the oxide. A well–cured silicon resin is used between and over the field plates that is essentially free from mobile charge [20]. This device is shown because of its relative insensitivity to surface charge. The device with an x_d/x_o ratio of 25.6 can be neglected because the data shows the device is well beyond breakdown. Breakdown occurs when the ionization integral (vertical axis) reaches 1. The peak value of the structure with ratio of 11.9 is not affected significantly by N_{ss}, and thus the breakdown of this region. However, there are some considerable differences on both sides of the peak with a relatively low surface–charge density

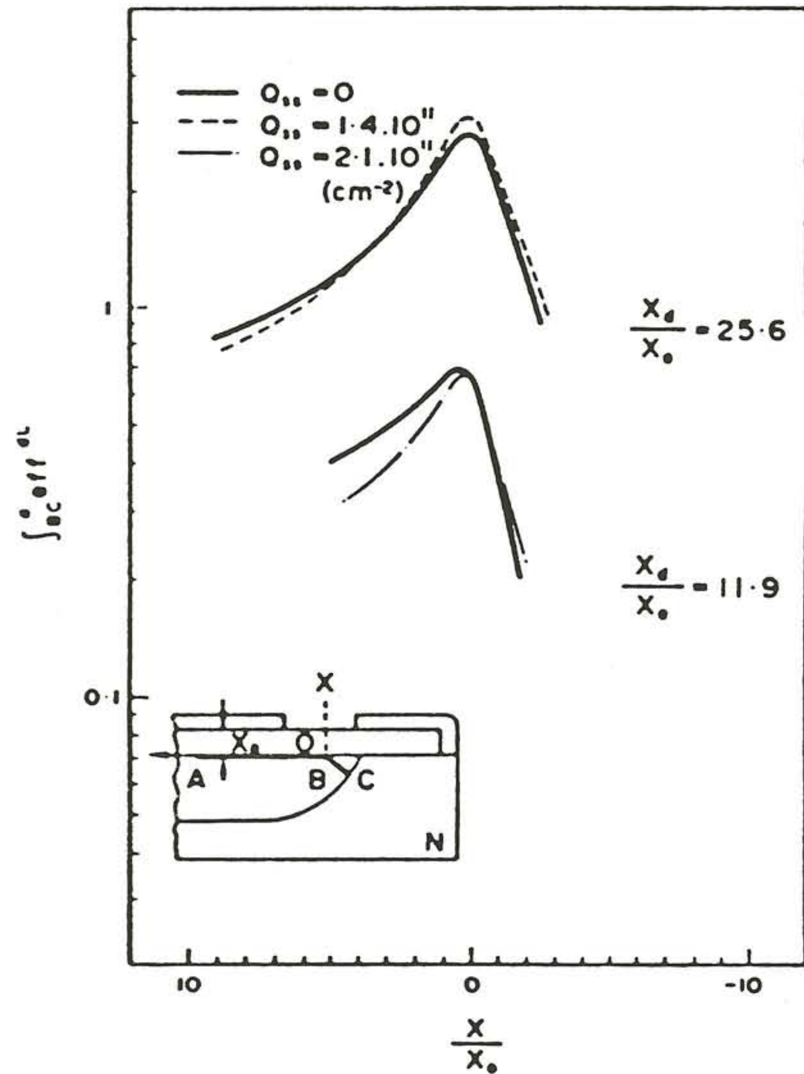


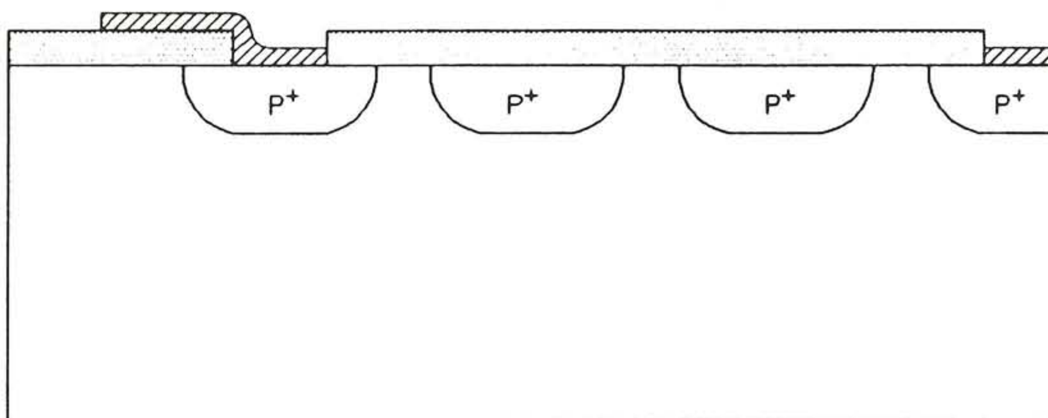
Figure 5-11. Ionization integral calculations for a field plate structure subjected to varying surface charges. (After Conti and Conti [19].)

$(2.1 \times 10^{11}\, cm^{-2})$. In this work, one needs to be interested in the effects of surface charges up to and above $10^{12}\, cm^{-2}$.

5.5 Structures with Field Rings and Field Plates

Instead of using a field plate alone on the main junction, it is more common to use a field plate in conjunction with floating field rings by placing the plate on the last floating ring or using a field plate on the main junction with floating rings beyond the junction as shown in Fig. (5-12). In Fig. (5-12a), the field plate is floating and has no external bias placed on it. With different surface charges, a different punch–through voltage will reach this last ring and plate. This potential will initially be a small amount, and with increased surface charge, punch–through to this last ring may not happen resulting in no potential on the field plate. In Fig. (5-12b), the potential on the field plate will always be the same no matter what the surface charge is because it is being externally biased.

By using these two methods in the same termination, one takes advantage of the benefits of both. These are favorable terminations that further the breakdown voltage from using just a planar junction. The effects of surface charge must be considered, too. It has been shown that results from field plates are uncertain to surface charge effects, and that a thick oxide layer is needed to make them effective. Very thin oxide layers are much less susceptible to surface charges, though. Therefore, power devices needed for radiation environments should have thin oxide layers and no field plates.



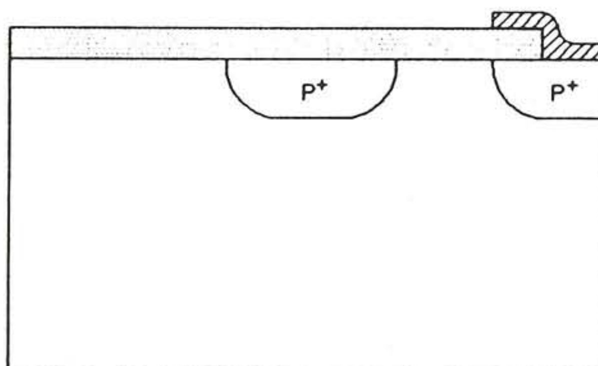


Figure 5-12. Termination structure using combinations of field rings and field plates: (a) floating field plate; (b) field plate on main junction. ((a) is after Baliga [11].)

CHAPTER 6

RESULTS OF SIMULATING TERMINATION STRUCTURES

In this chapter, results from simulating certain device termination structures will be presented. As was discussed in Chapter 4, these simulations are made with the SEPSIP [53,68] computer program which solves for the electrostatic potential and electric field distributions. The code is written in FORTRAN for a VAX environment. SEPSIP creates a drawing interchange file (.DXF) which AutoCAD [7] uses to draw the equipotential lines, equifield lines, and maximum electric field locations (small circles). A majority of the simulations are made with a Digital Equipment Corporation MicroVAX 3600 mainframe whose simulation times range from 5 minutes for simple structures to 25 minutes for more complex structures. These times are for the numerical calculations only. Added to these times would be the amount of time needed to transfer the .DXF file to an IBM PC (or compatible) to be used with AutoCAD. Again, these times vary from 3 to 15 minutes. If one was interested only in the output files (.OUT and .PTH) created by SEPSIP and not the .DXF file, then the times given above would be accurate.

The goal of these simulations is threefold. First, it is desired to verify that the code is performing properly. These verifications are made by simulating simple structures to which known solutions exist. Varying such parameters as surface–charge density and doping concentration in these simple structures test the code to see if appropriate results are produced. Also, by simulating simple structures, one has a much better idea as to what qualitative results should occur. Secondly,

verifying that these proper results do occur leads to simulating more complex structures to see if they behave similarly and somewhat qualitatively as expected. These comparisons are made with devices that have been built and subjected to physical experiments. The potential distributions in these existent devices cannot be monitored, but such things as breakdown voltage can be compared to the simulations. Thirdly, with results from the above types of simulations, the code can be used to find the optimal device for a certain application. In this work, a device relatively insensitive to varying surface charge and possessing as high a breakdown voltage as possible is sought. The size of the device is not specified, but a practical limit exists when a slight gain in breakdown voltage occurs for a significant change in size.

6.1 One–Dimensional Abrupt Junction

The first arbitrary device termination structure considered is a one–dimensional semi–infinite np^+ junction diode as was shown in Fig. (3-3). This structure is presented first because it possesses the highest breakdown voltage and will be considered as the "optimal" breakdown voltage for an np^+ junction with a specific doping profile. The substrate impurity concentration is approximately $1 \times 10^{15}\, cm^{-3}$. Doping profiles in fact were obtained from spreading resistance measurements made on an existent device [63]. The profile is approximately Gaussian with a surface concentration of $1 \times 10^{18}\, cm^{-3}$ as shown in Fig. (6-1). The same doping profile was used for the junctions and field rings in all devices examined in this work.

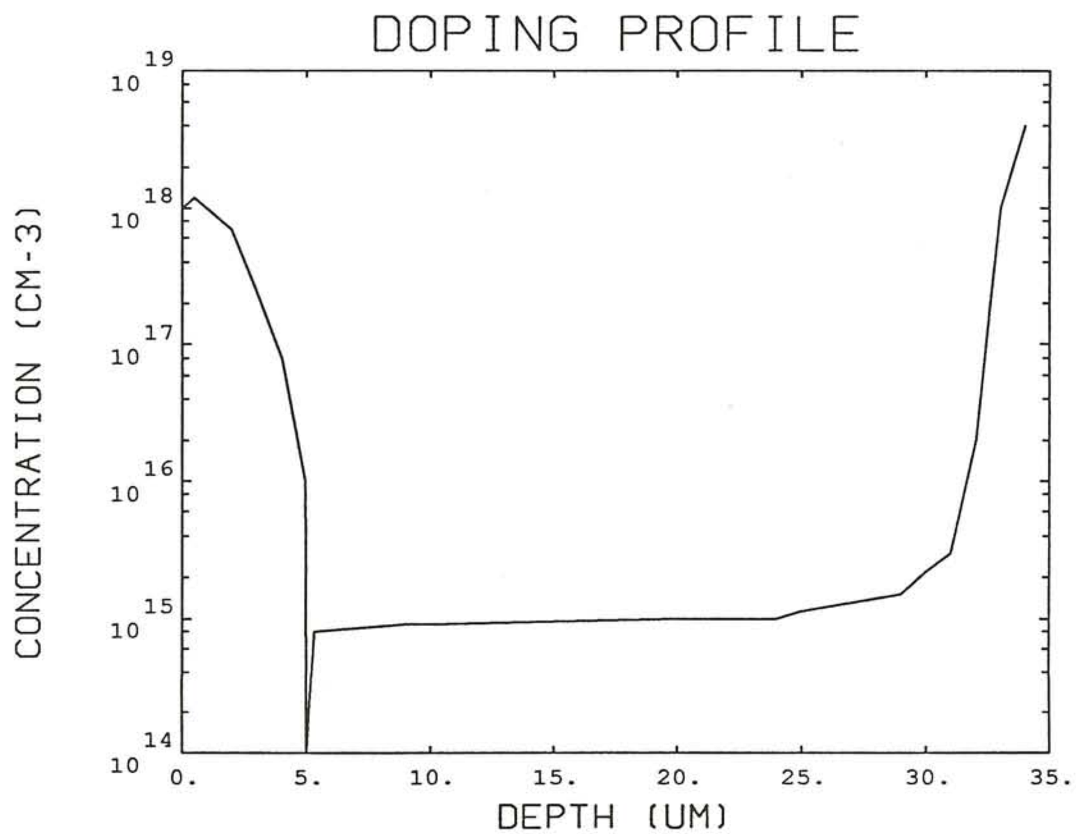


Figure 6-1. Gaussian doping profile used in the simulations for the junctions and field rings.

Results of the SEPSIP simulation calculated the breakdown voltage to be $327\,V$ with an electric field maximum E_{max} of $0.30 \times 10^6\,V/cm$. Using the one-dimensional abrupt junction breakdown voltage equation (Eq. (3-25)),

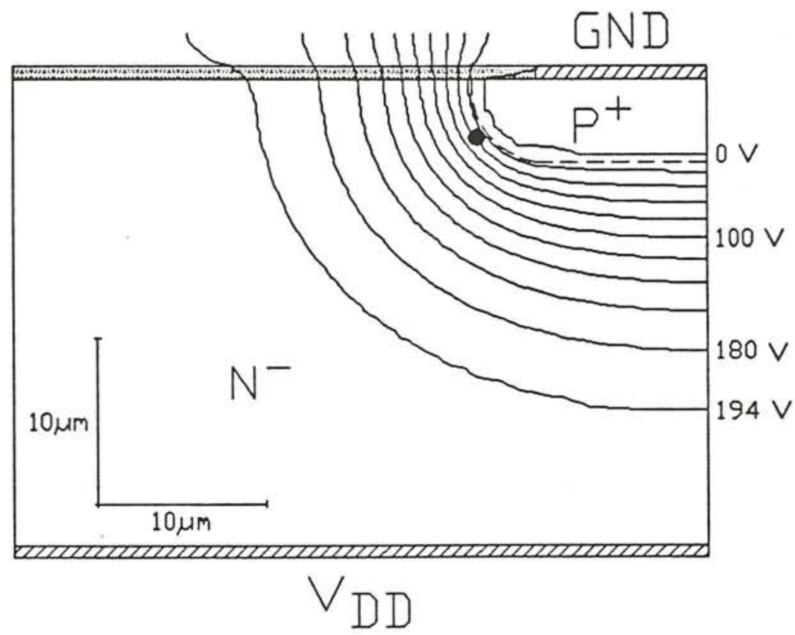
$$V_B = \frac{\epsilon\, E_{max}^2}{2\, q\, N_{BC}} \qquad (6-1)$$

where ϵ is the permittivity, E_{max} is the maximum electric field, q is the elementary charge, and N_{BC} is the background (substrate) doping concentration, breakdown can be approximated. Using an N_{BC} of $0.9 \times 10^{15} cm^{-3}$ in Eq. (6-1), yields a breakdown voltage of $324\,V$. This is only less than a 1% difference from the $327\,V$ indicating that the code gave very good qualitative results.

6.2 Planar Diffused Junction

Next, a somewhat shallow planar–diffused junction was simulated. Fig. (6-2a) shows a cross section of this structure with equipotential lines calculated by SEPSIP superimposed. The junction depth is $5\,\mu$m, the oxide thickness is $0.7\,\mu$m, N_{ss} is zero, and the same doping profile mentioned in the previous section (Fig. (6-1)) is used. The solid circle in Fig. (6-2a) shows the location of the peak electric field. The value of the field is $0.35 \times 10^6\,V/cm$. Calculation of the multiplication factor along the ionization path indicated that breakdown occurred for a reverse-bias voltage of $194\,V$.

Fig. (6-2b) shows the same cross section except that the device was simulated with $N_{ss} = 1 \times 10^{12}\,cm^{-2}$. Because the net charge in the oxide has been taken to be positive, the carrier density in the N^- region near the surface increases. This causes a decrease in depletion layer width and the crowding of the potential lines at the surface. The solid circle, again, shows the peak electric field location which has been moved to the surface. This location of the peak electric field results



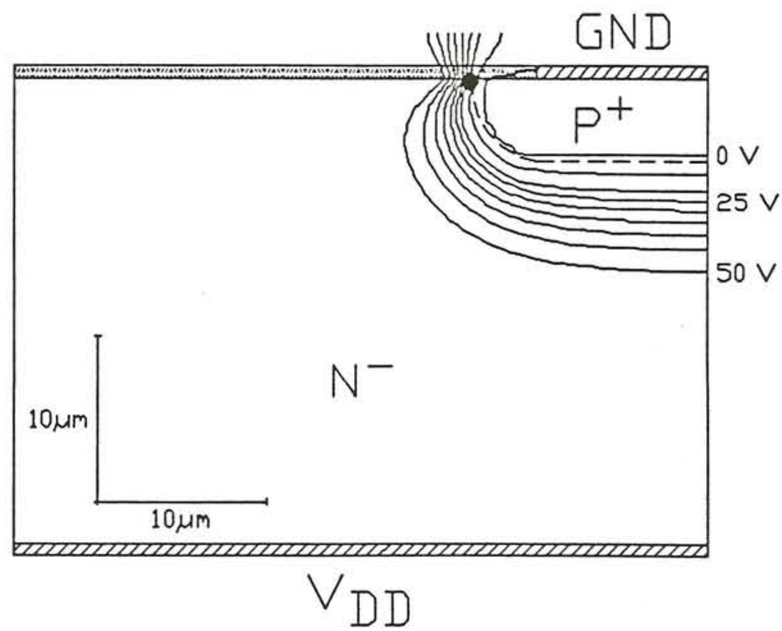


Figure 6-2. Potential distribution for simple two–dimensional *p-n* junction. (a) $N_{ss} = 0\,cm^{-2}$. (b) $N_{ss} = 1 \times 10^{12}\,cm^{-2}$.

in a drastic reduction in breakdown voltage. It broke down at a voltage of $92\,V$ which means that this devices is very instable to surface–charge variations. A plot of breakdown voltage versus surface–charge density for this device can be found as the curve labeled "0 Rings" in Fig. (6-7).

With zero surface charge, the device broke down at a relatively low voltage ($194\,V$), though. $194\,V$ is only 59% of the optimal $327\,V$ that might be achieved. Since it is desired to design a structure that possesses a high breakdown voltage, preferably close to the optimal breakdown voltage, this planar diffused termination structure needs to be improved. In the following sections, methods of changing this planar junction to improve junction characteristics shall be discussed.

6.3 Floating Field Ring Termination

The first technique considered to improve the breakdown voltage is the addition of one floating field ring optimally spaced from the main junction. This device, with the potential distribution for $N_{ss} = 0$, is shown in Fig. (6-3) where optimal spacing is achieved because the high electric field spots (circles) appear on both junction curvatures simultaneously. From the computer simulations, it was verified that this spacing resulted in the highest breakdown voltage. This optimal spacing was $9.5\,\mu\mathrm{m}$ between rings after lateral diffusion. Figure (6-8), where breakdown voltage of this one-ring device is plotted against surface charge, indicates that for $N_{ss} = 9 \times 10^{11}\,cm^{-2}$ or greater, the breakdown curve followed that of the zero–ring device. This happened because punch–through to the field ring did not take place before breakdown at this value of N_{ss}.

As mentioned in Section 5.2, the electric field crowding is least when similar electric fields occur on the ring and main junction at the same time. This leads to

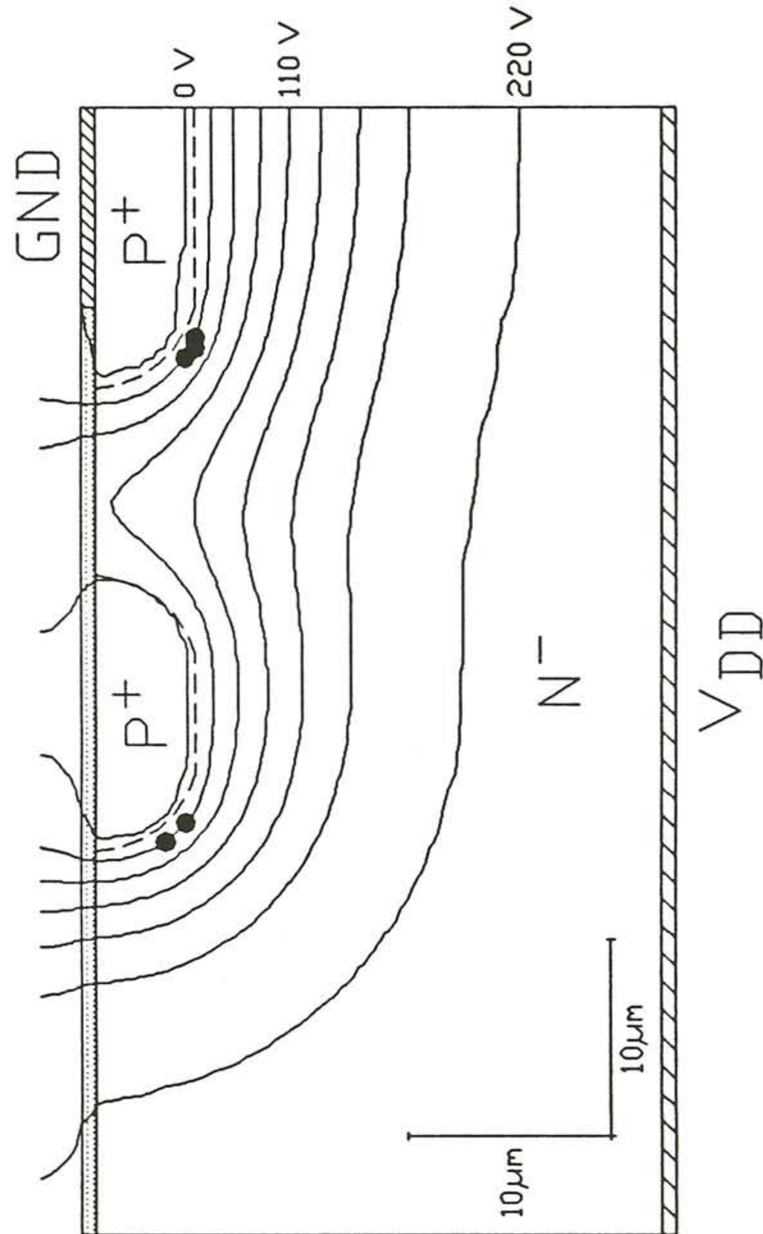


Figure 6-3. Potential distribution for one-ring termination structure ($N_{ss} = 0\,cm^{-2}$).

impact ionization taking place on these two junctions concurrently. This theoretical claim was verified by the code which computed the greatest breakdown voltage for this spacing. A plot of breakdown voltage versus ring spacing for $N_{ss} = 0\,cm^{-2}$ (Fig. (6-4)) yields a Gaussian–like distribution with the peak occurring for the 9.5–μm spacing. The spacing is very sensitive in determining optimality.

6.4 Multiple Floating Field Ring Terminations

A higher breakdown voltage was attained for a three–ring structure. The depletion region of this device, shown in Fig. (6-5), is spread out considerably as compared to structures already presented. This leads to less of an electric field present in this region and the ability to bias the device with a higher voltage. The spacing of the rings was kept fixed in determining the optimal spacing in this three–ring device. It was found that this distance was $7.5\,\mu$m and this device structure is shown in Fig. (6-5), with the overlaid potential distribution simulated for $N_{ss} = 0$. As shown in Fig. (6-8), this device broke down at $278\,V$ with an N_{ss} of zero. Again, the sharp bends plotted in this curve are a result of the punch–through phenomenon not reaching a ring before breakdown occurred for increased amounts of surface charge.

As mentioned above, the spacing of the rings in this device was kept fixed. Because of this, the highest electric field locations appeared on the main junction and last ring only, as shown in Fig. (6-5). Brieger, *et al* [16] observed the same results with three equally spaced rings as shown in their three–dimensional electric field distribution of Fig. (6-6). They claim that the inner rings are not completely exploited which is also a conclusion that can be based on the results of this work. Increasing the spacing of the outer rings would increase the breakdown voltage.

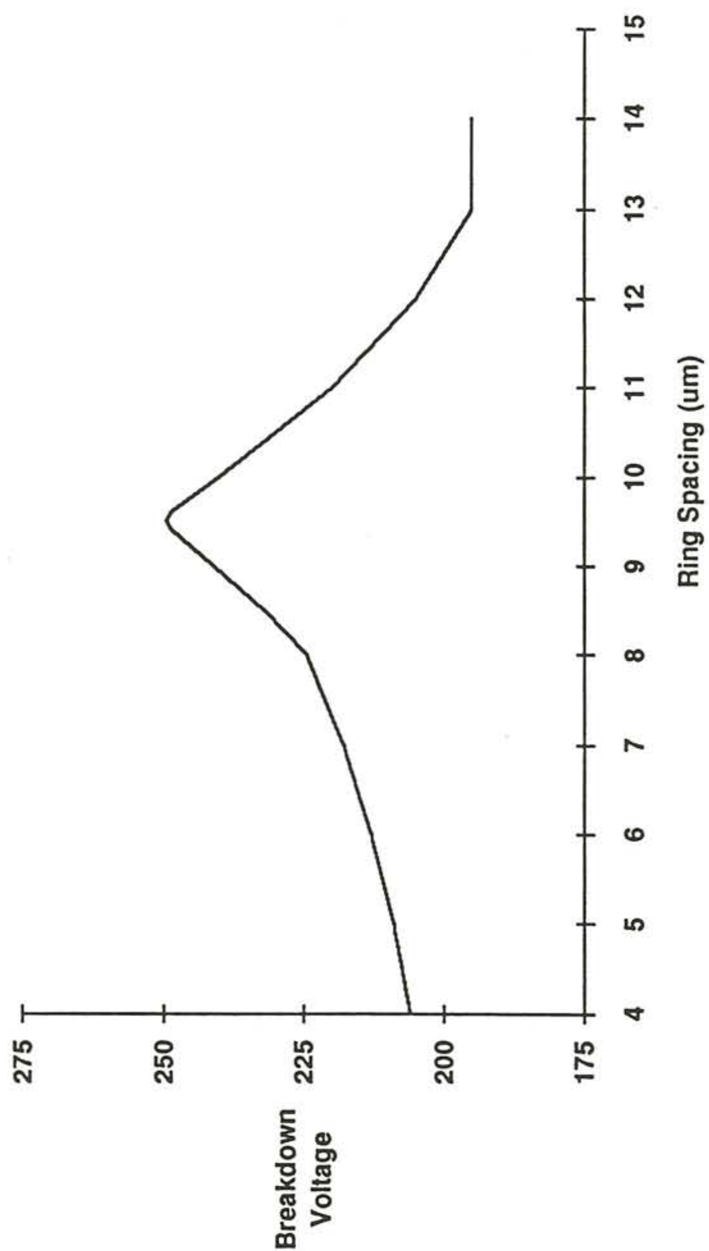


Figure 6-4. Breakdown voltage versus ring spacing for a one–ring termination structure device ($N_{ss} = 0\,cm^{-2}$).

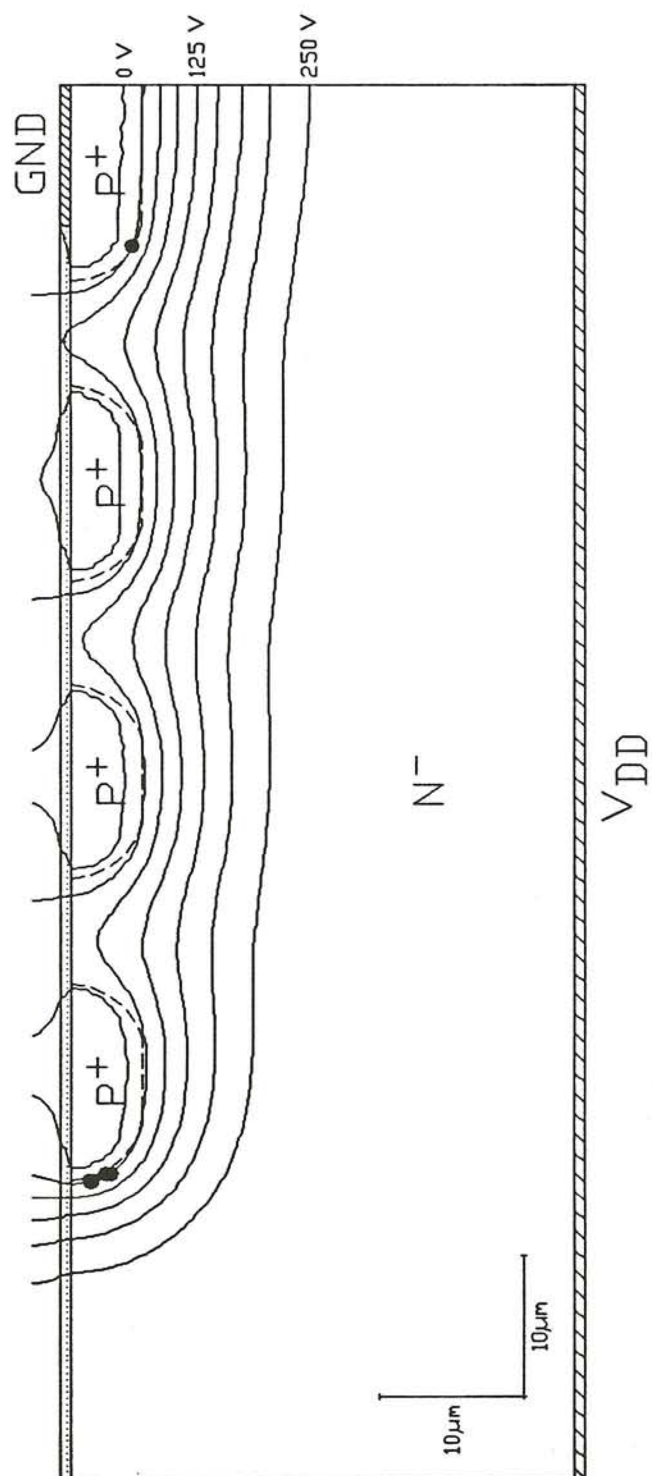


Figure 6-5. Potential distribution for three-ring termination structure ($N_{ss} = 0\,cm^{-2}$).

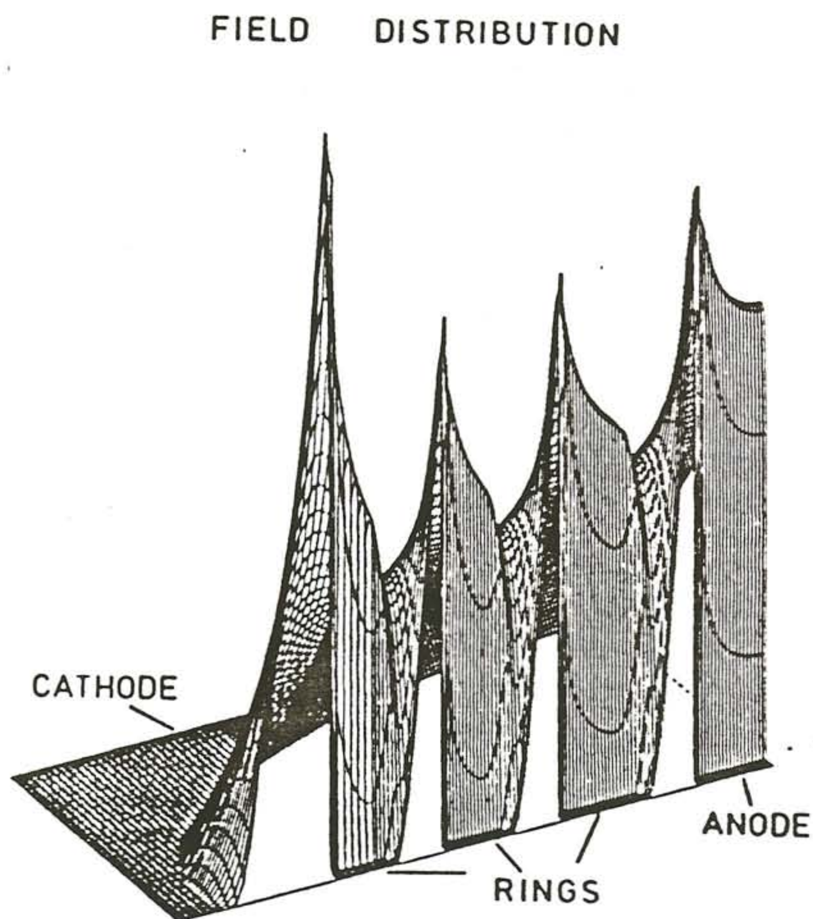


Figure 6-6. Three–dimensional electric field distribution for an equally spaced three–ring termination structure. (After Brieger, *et al* [16].)

Through simulation, it was found that allowing variable ring spacing increased the breakdown voltage characteristics of a device having more than one ring. For avalanche breakdown to occur on all rings simultaneously, the spacing between different pairs of rings had to vary slightly. The seven–ring breakdown curve in Fig. (6-8) is for a device with this type of spacing. Fig. (6-7) shows this device, with the potential distribution for $N_{ss} = 0$, where the spacing between the first ring and the main junction is $2.0\,\mu$m, increasing to $12.0\,\mu$m between the last pair of rings. In this figure, a somewhat optimal spacing of the rings is achieved because of the peak electric fields appearing on different rings. The two outer rings actually are too far from the third to last ring. The fourth ring from the main junction, the one with three peak fields, should be moved a little farther from the third ring so that the crowding of the electric field in this area can be reduced. These changes would lead to an increase in breakdown voltage of only a few percent, though.

The seven–ring structure is shown because this device was fabricated and experimental measurements were made on the device [63]. The analysis indicated no degradation of the $268\,V$ breakdown voltage for radiation levels up to 1 MRad(Si). SEPSIP calculated the breakdown voltage to be $281\,V$ which is in error by only 5%. From the potential distribution in Fig. (6-7), it can be seen that the depletion layer depth below each ring gradually decreases as one moves farther from the main junction. The potential difference between a ring and the bulk material decreases as the distance of the ring from the main junction increases. This gradual decrease in depletion layer depth causes the termination to look similar to a parallel–plane junction. Again, the lower boundary of the depletion region around the last ring indicates that this ring is too far from the previous ring. The 250–V equipotential line should not bend in the space between these two outer rings.

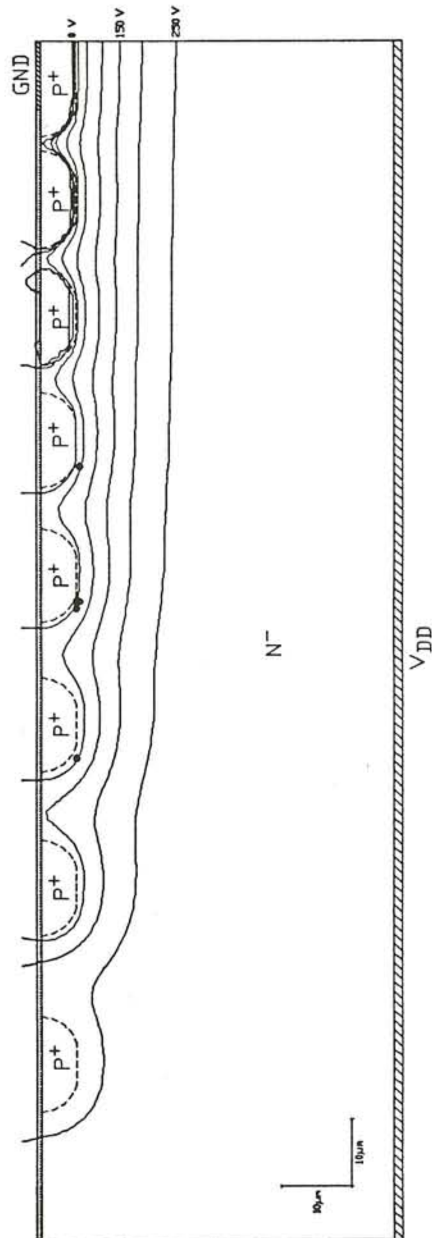


Figure 6-7. Potential distribution for seven–ring termination structure (N_{ss} = $0\,cm^{-2}$).

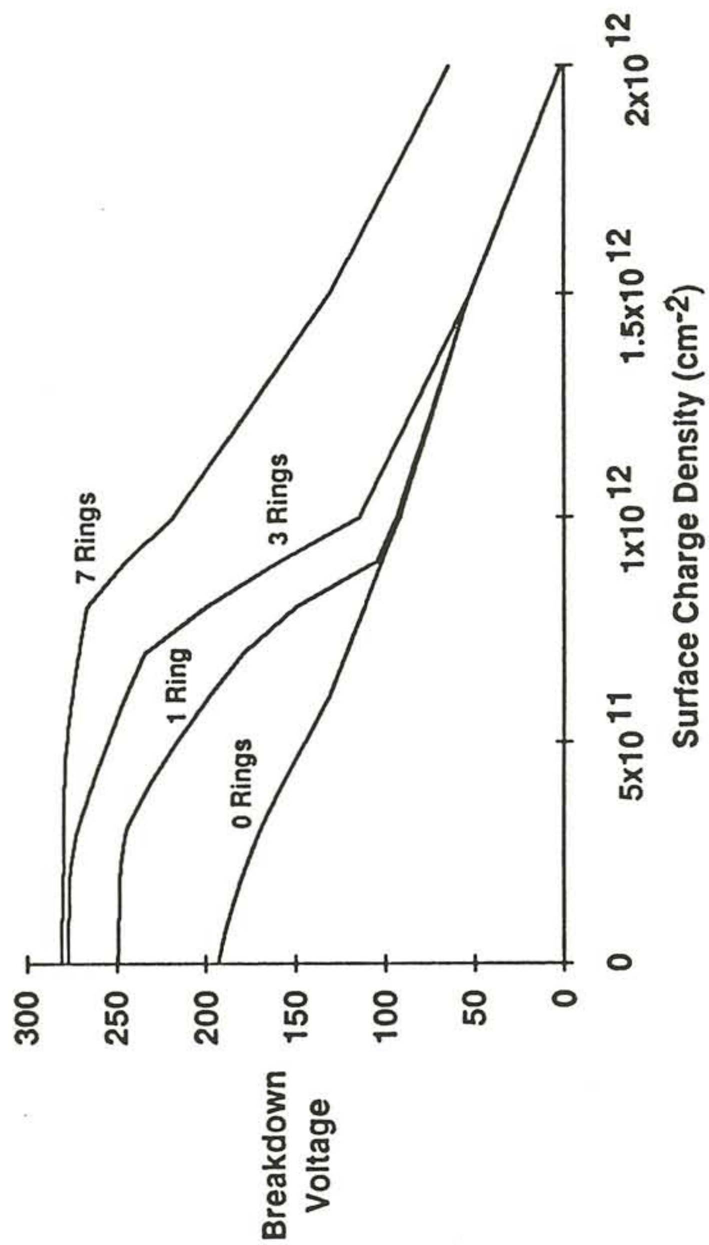


Figure 6-8. Breakdown voltage versus surface–charge density for various numbers of floating ring structures.

The measured breakdown voltage of a six–ring structure is plotted versus surface–charge density in Fig. (6-9). A diagram of the device cannot be shown in this text, but it employs the design rule of variable ring spacing described above. Each data point in Fig. (6-9) represents the average of six samples. The total dose has been converted to surface–charge density using the formula described in Chapter 2,

$$N_{ss} = D\,t_{ox}\,G\,F \qquad (6-2)$$

where D is the total dose, t_{ox} is the oxide thickness, G is the generation rate of electron–hole pairs per unit volume, and F is the fraction of holes transported and trapped at the interface [33]. Using an appropriate F in this simple model ($F = 0.001$) to calibrate the experimental data to the simulation, good qualitative agreement was found. A hardened field oxide was used in this device so a value of 0.1% for F is not considered unusual [63]. A more sophisticated model or additional experiments could be used to establish more precisely the relation between total dose and surface–charge density if required. In most situations, however, it is sufficient to minimize the dependence of breakdown voltage on surface–charge density. The use of a hardened field oxide, or reducing oxide thickness, will reduce the amount of charge buildup as a function of total dose.

6.5 Equipotential Field Plate Terminations

A termination structure with only a field plate is shown in Fig. (6-10) with the SEPSIP calculated potential distribution imposed over the device. For this structure to be effective in spreading out the depletion layer at the surface, a relatively thick oxide layer had to be used. This oxide is 2.0 μm thick compared to 0.7 μm oxide layer thicknesses used in the field ring devices.

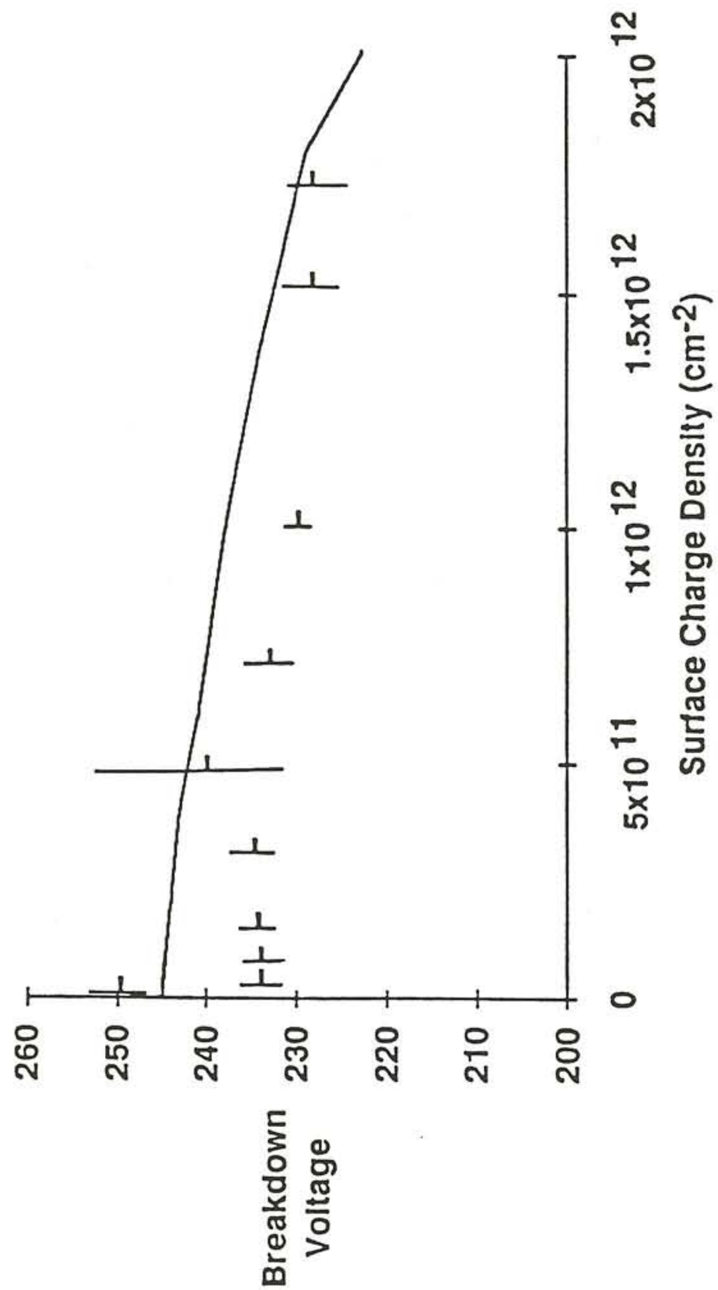


Figure 6-9. Breakdown voltage versus surface–charge density for a six–ring termination structure. Each data point represents the average of six samples. Line represents simulation results.

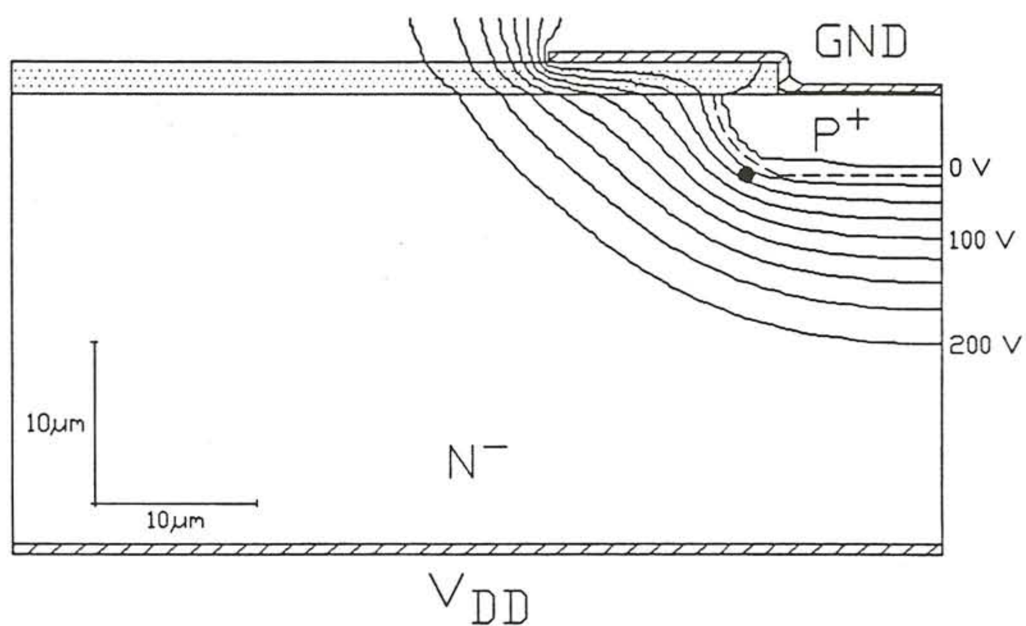


Figure 6-10. Potential distribution for field plate termination structure ($N_{ss} = 0\,cm^{-2}$).

The effects of surface charge on this structure is compared to a planar structure in Fig. (6-11). With the much thicker oxide layer, the surface charge will accumulate much faster than the thinner oxide layer. Referring to Eq. (6-2), N_{ss} is directly related to oxide thickness and will be nearly three times as great for this structure with the same total dose.

6.6 Terminations With Field Rings And Field Plates

In Fig. (6-12a), a device terminated with a floating field ring with attached field plate is shown. With these two techniques in the same device, a much smoother lower depletion region boundary is obtained as can be seen by the 250–V line. This leads to an initial breakdown voltage higher than that of a one-ring structure. The advantage of the field plate disappeared with increased surface charge, though. This is due to the fact that punch–through does not occur for higher charge densities and the plate has no effect (Fig. (6-12b)). These results are presented in Fig. (6-13) where a comparison of this plate structure is made with the one–ring structure that does not use a field plate.

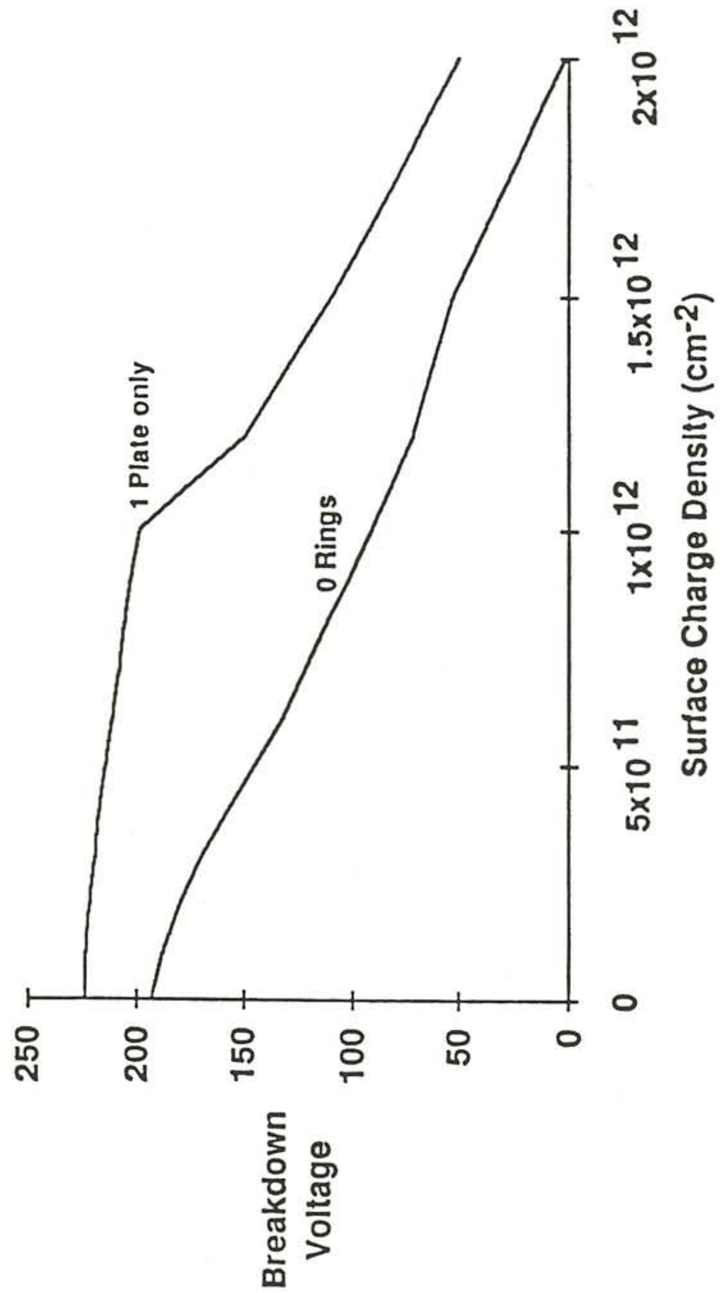
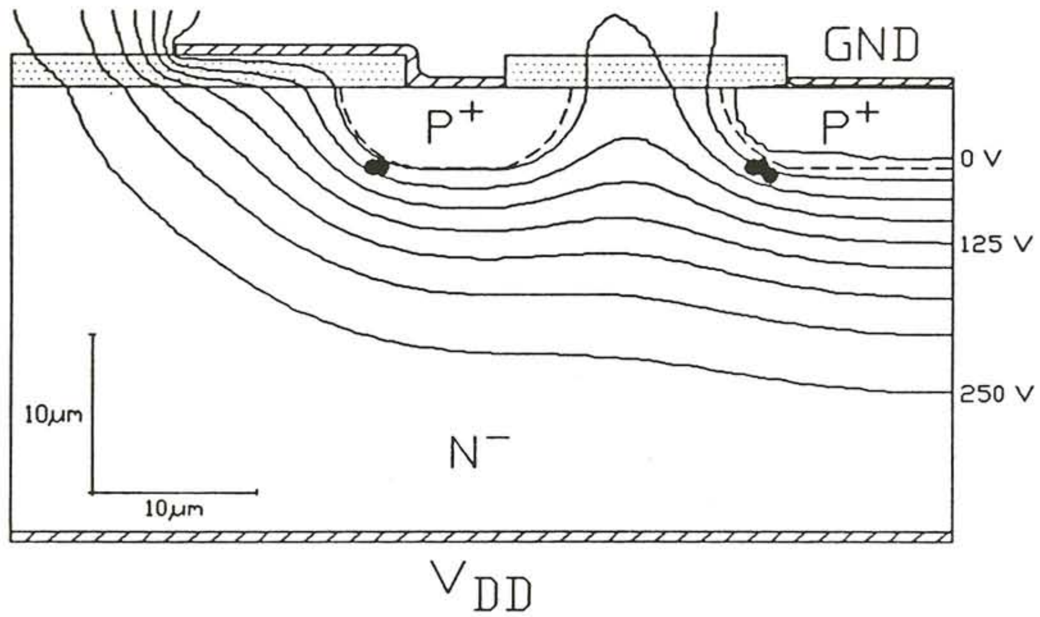


Figure 6-11. Breakdown voltage versus surface–charge density for field plate termination structure.



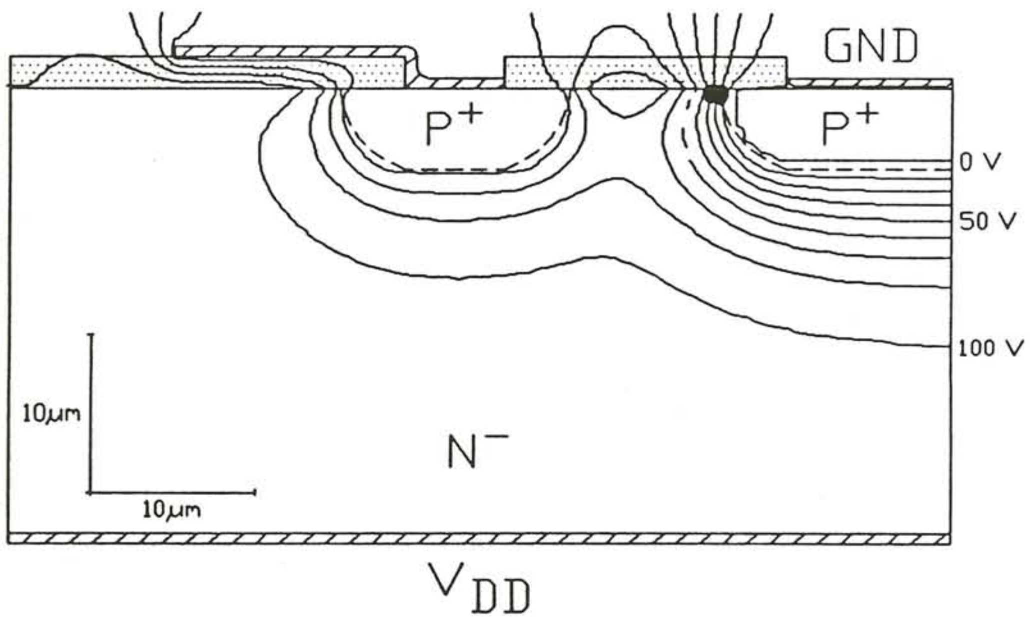


Figure 6-12. Potential distribution for combination ring/plate termination structure. (a) $N_{ss} = 0\,cm^{-2}$. (b) $N_{ss} = 1 \times 10^{12}\,cm^{-2}$.

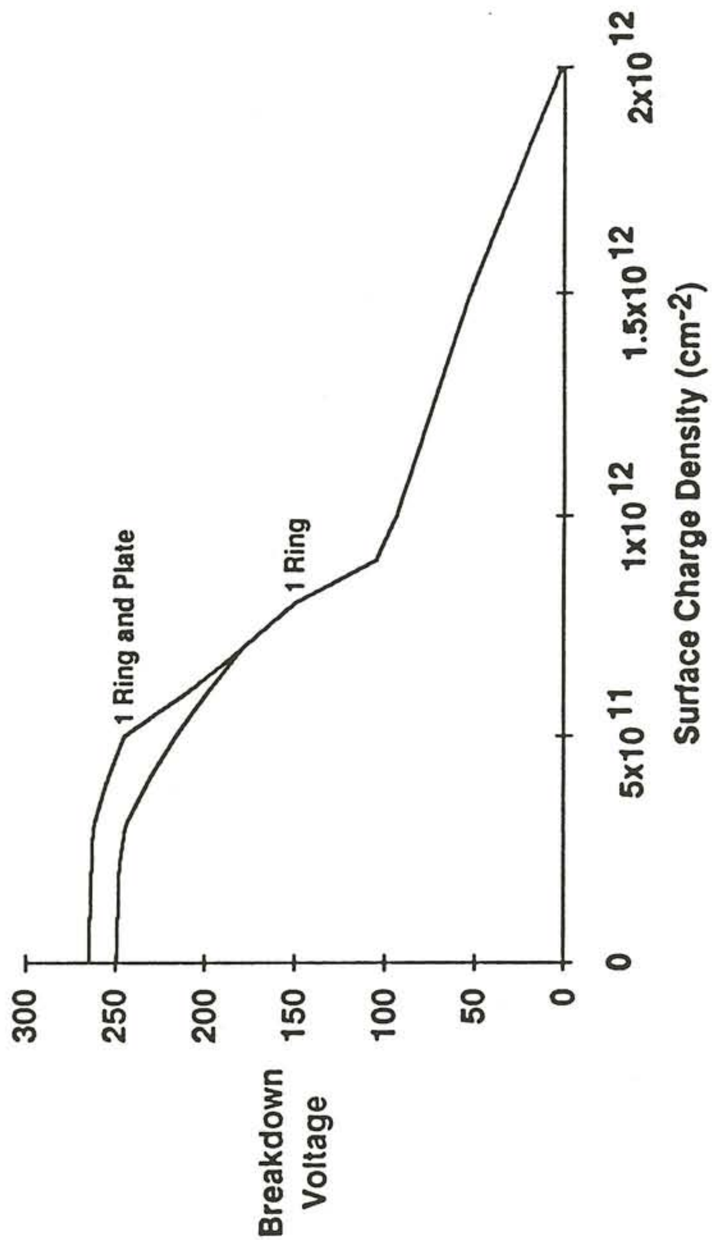


Figure 6-13. Breakdown voltage versus surface-charge density for combination ring/plate termination structure.

CHAPTER 7
RESULTS OF APPROXIMATING PUNCH–THROUGH VOLTAGES IN FIELD RING DEVICES

Figure (5-7) showed the depletion layer punching–through to a floating field ring when surface charge was present. Because the SEPSIP code does not yet compute this automatically, a means of calculating these punch–through voltages is needed. The punch–through voltage is a function of three items; the ring spacing, the surface–charge density present at the interface, and substrate impurity concentration present at the surface. Through simulation and the depletion layer width equation (Eq. (3-23)), some type of punch–through voltage equation can be derived. This section is dedicated to correlating experimental data to this type of equation. In this work, the surface doping concentration was kept at a constant $1 \times 10^{15}\, cm^{-3}$. A function was found for punch–through voltage as a function of the other two variables. The following section describes how this equation was found.

7.1 Mathematical Approximations

When no surface charge is present, the following method can be used to determine the punch–through voltage between rings (punch–through will occur at the surface): First, each reverse–biased *p-n* junction has an intrinsic (built–in) voltage (ΔV) of approximately 0.7 to 0.8 V. In this work, 0.75 V has been chosen to represent this potential. For silicon, computing the depletion width in the one–dimensional equation [61]

$$W = \sqrt{\frac{2\,\epsilon_s\,(V + \Delta V)}{q\,N_D}} \qquad (7-1)$$

with $\Delta V = 0.75\,V$ and N_D approximately $1 \times 10^{15}\,cm^{-3}$ yields a built–in depletion width of $1\,\mu$m that exists around a floating field ring. If the adjacent ring is $2\,\mu$m from this ring, then both depletion regions around the rings would be touching at the surface and no potential difference between the rings would be needed to punch one depletion layer through to the next. Similarly, the potential needed on a ring is such to make the depletion region extend to the next ring minus the $1\,\mu$m. Rearranging Eq. (7-1) yields

$$V_{PT} = \frac{W^2\,q\,N_D}{2\,\epsilon_s} - \Delta V \qquad (7-2)$$

so that the punch–through voltage is a function of the width the depletion layer must extend to reach the next ring. The punch–through voltages readily can be calculated using this one–dimensional equation when the width between rings is known.

It becomes more complicated when surface charges must be considered. The following method is a good approximation for determining the punch–through voltage when surface charge exists. This is true because the results of these calculations were used with SEPSIP and the code showed the depletion layer to extend very close to the built–in depletion region around the adjacent ring. SEPSIP produced output similar to Fig. (6-2b) to show the punch–through below the surface. First, the Debye length is calculated from the equation [61]

$$L_D = \sqrt{\frac{\epsilon_s\,k\,T}{q^2\,N_D}} \qquad (7-3)$$

for the known impurity concentration at the surface. In Eq. (7-3), k is Boltzmann's constant ($1.380 \times 10^{-23}\,J/K$) and T is the temperature in Kelvin. The positive surface charge at the interface causes an increase in n–type impurities at the surface

similar to what is shown in Fig. (5-4). A new impurity concentration at the surface is thus taken to be the sum of the concentration already present (N_D) plus N_{ss}/L_D. This new value for N_D is then used in Eq. (7-1) to calculate a new built–in depletion layer width around a ring. This new value of W is used with the old value of N_D in Eq. (7-2) to produce a value for the punch–through voltage. Punch–through now will occur below the surface where the impurity concentration is not altered.

For this work, a constant surface impurity concentration of $1 \times 10^{15}\ cm^{-3}$ is used. In Table (7-1), the punch–through voltages are shown when the other two variables are allowed to change. Ring spacings are shown across the top and surface–charge density values are shown at the left. Also, the punch–through voltage is plotted versus surface–charge density in Fig. (7-1) with each curve representing a constant ring spacing. In addition, Fig. (7-2) shows punch–through voltage versus ring spacing where each curve represents a constant surface–charge density this time. It is desired to express these curves mathematically, and also, in one combined equation. Therefore, the following steps were taken to produce this type of equation.

The curves in Fig. (7-2) are assumed to be described by the equation

$$V_{PT} = a(N_{ss}) \cdot x^2 + b(N_{ss}) \cdot x + c(N_{ss}) \qquad (7-4)$$

because of their quadratic nature. In Eq. (7-4), x is the ring spacing and a, b, and c are functions of N_{ss} to be determined because V_{PT} is also a function of N_{ss}. A matrix of equations can be set up to determine these a, b, and c functions because the V_{PT}'s and ring spacings (x's) are known.

$$\begin{bmatrix} V_{PT_{1\,1}} & V_{PT_{1\,2}} & \cdots & V_{PT_{1\,16}} \\ V_{PT_{2\,1}} & V_{PT_{2\,2}} & \cdots & V_{PT_{2\,16}} \\ \vdots & \vdots & \ddots & \vdots \\ V_{PT_{15\,1}} & V_{PT_{15\,2}} & \cdots & V_{PT_{15\,16}} \end{bmatrix} = \begin{bmatrix} x_1^2 & x_1^1 & 1 \\ x_2^2 & x_2^1 & 1 \\ \vdots & \vdots & \vdots \\ x_{15}^2 & x_{15}^1 & 1 \end{bmatrix} \cdot \begin{bmatrix} a_1 & a_2 & \cdots & a_{16} \\ b_1 & b_2 & \cdots & b_{16} \\ c_1 & c_2 & \cdots & c_{16} \end{bmatrix} \qquad (7-5)$$

	A	B	C	D	E	F	G	H	I
1	Nss \ x	2 um	3 um	4 um	5 um	6 um	6.5 um	7 um	7.5 um
2	0	0	2.25	6	11.25	18	21.9375	26.25	30.9375
3	1E+10	0.422	3.047	7.172	12.797	19.922	24.047	28.547	33.422
4	5E+10	1.044	4.114	8.683	14.753	22.323	26.67	31.393	36.49
5	1E+11	1.32	4.563	9.305	15.547	23.289	27.723	32.532	37.715
6	2E+11	1.556	4.936	9.816	16.197	24.077	28.579	33.457	38.71
7	3E+11	1.671	5.116	10.061	16.506	24.451	28.986	33.896	39.181
8	4E+11	1.742	5.227	10.211	16.696	24.68	29.235	34.165	39.469
9	5E+11	1.792	5.304	10.316	16.828	24.839	29.408	34.351	39.669
10	6E+11	1.83	5.362	10.394	16.926	24.958	29.537	34.49	39.819
11	7E+11	1.859	5.407	10.455	17.003	25.051	29.637	34.599	39.935
12	8E+11	1.883	5.444	10.505	17.066	25.126	29.719	34.687	40.03
13	9E+11	1.903	5.475	10.546	17.118	25.189	29.787	34.76	40.109
14	1E+12	1.921	5.501	10.582	17.162	25.243	29.845	34.823	40.176
15	1.5E+12	1.979	5.59	10.701	17.313	25.424	30.042	35.035	40.403
16	2E+12	2.014	5.644	10.774	17.403	25.533	30.161	35.163	40.54
17	3E+12	2.057	5.708	10.86	17.512	25.663	30.302	35.315	40.703

	J	K	L	M	N	O	P
1	8 um	8.5 um	9 um	9.5 um	10 um	11 um	12 um
2	36	41.4375	47.25	53.4375	60	74.25	90
3	38.672	44.297	50.297	56.672	63.422	78.047	94.172
4	41.963	47.81	54.032	60.63	67.602	82.672	99.242
5	43.274	49.208	55.516	62.2	69.258	84.501	101.243
6	44.337	50.34	56.717	63.47	70.597	85.978	102.858
7	44.841	50.876	57.286	64.07	71.23	86.675	103.62
8	45.149	51.204	57.633	64.438	71.618	87.102	104.087
9	45.363	51.431	57.874	64.693	71.886	87.398	104.41
10	45.522	51.601	58.054	64.883	72.086	87.618	104.65
11	45.647	51.733	58.195	65.031	72.243	87.79	104.838
12	45.748	51.841	58.309	65.151	72.369	87.93	104.991
13	45.832	51.93	58.403	65.251	72.475	88.046	105.117
14	45.904	52.006	58.484	65.337	72.564	88.145	105.226
15	46.146	52.265	58.758	65.626	72.869	88.48	105.591
16	46.293	52.42	58.922	65.8	73.052	88.682	105.811
17	46.467	52.605	59.118	66.007	73.27	88.922	106.073

Table 7-1. Punch–through voltage as a function of ring spacing and surface–charge density. Ring spacings are across the top and surface–charge densities are in the first left–hand column. N_{BC} = a constant $1 \times 10^{15}\ cm^{-3}$.

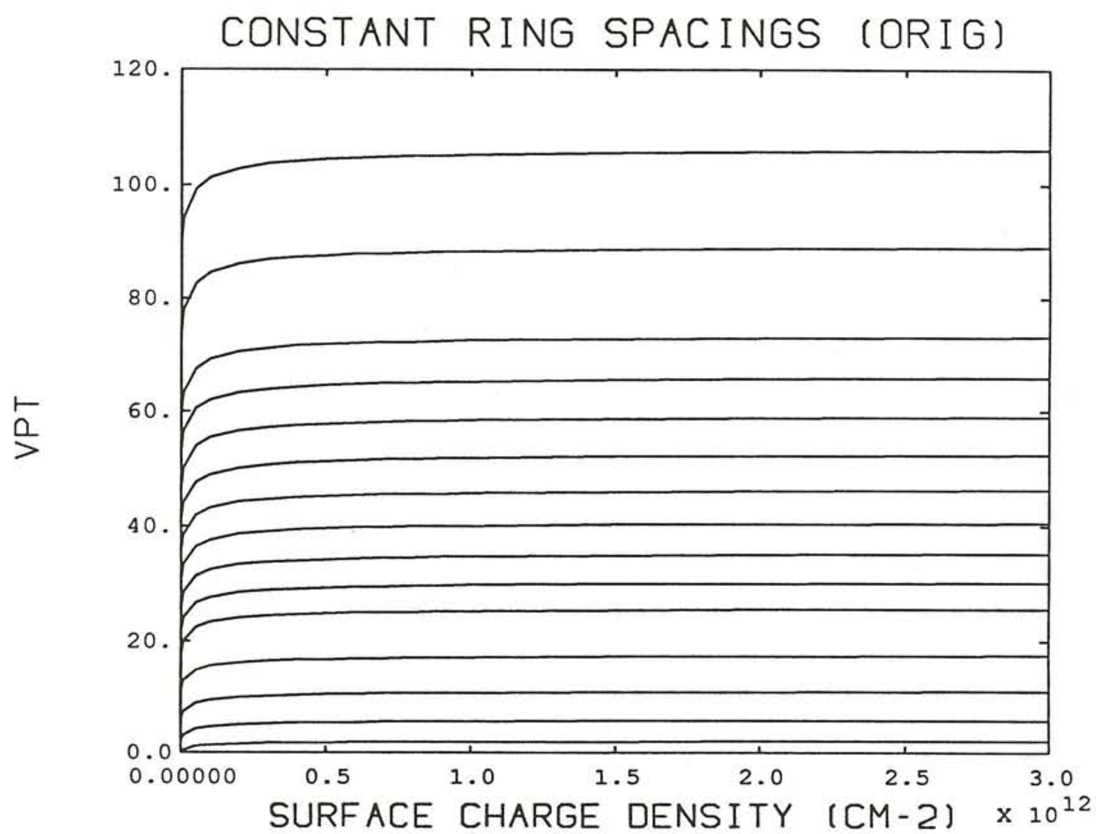


Figure 7-1. Punch–through voltage versus surface–charge density for constant ring spacings. This is experimental (simulation) data. Bottom curve is for 2-μm and the top curve is for 12-μm spacing.

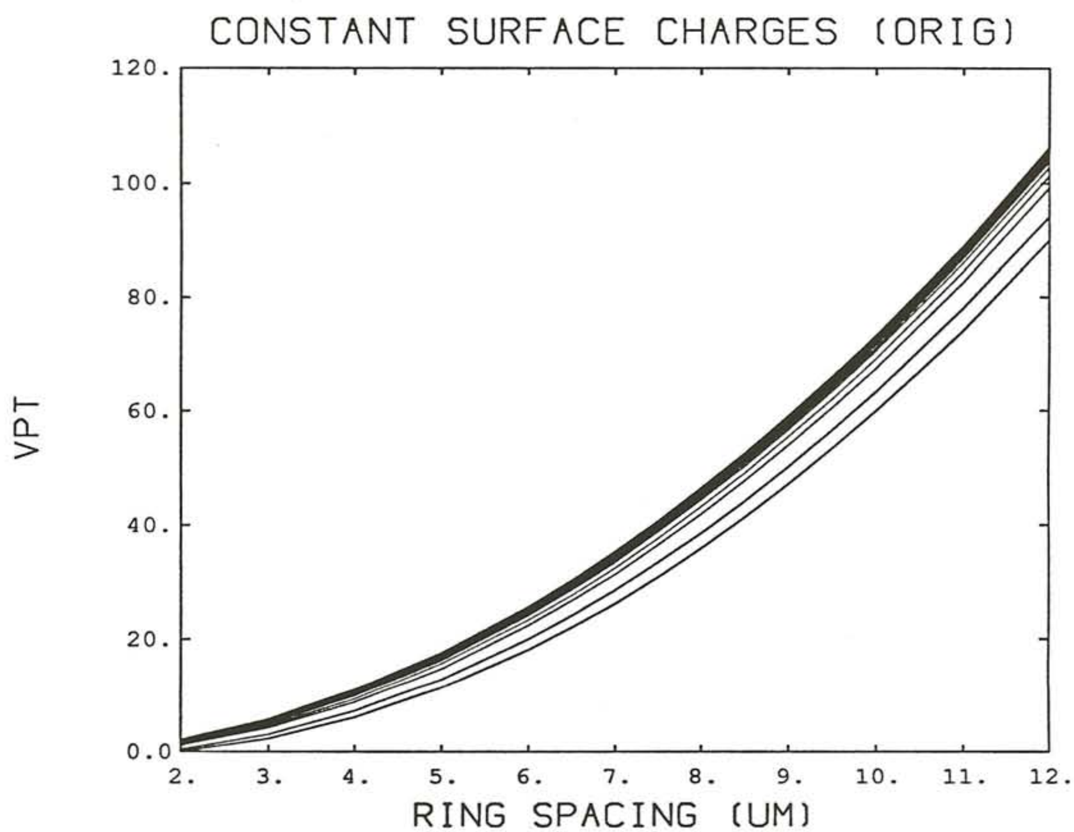


Figure 7-2. Punch–through voltage versus ring spacing for constant surface–charge densities. This is experimental (simulation) data. Bottom curve is for $0\,cm^{-2}$ and the top curve is for $3 \times 10^{12}\,cm^{-2}$ surface–charge density.

All of the a values turned out to be a constant 0.75. These occurred because of the choice of $0.75\,V$ for ΔV. Functions resulted for b and c, though. The solid line in Fig. (7-3) shows the experimental value for the b function and the dashed line is the curve–fitted line. Explanations of how the curve–fitted line was computed will be forthcoming in this section. Similarly, the solid line and dashed line in Fig. (7-4) are the experimental and curve–fitted lines for the c function, respectively. Through experimentation, the b and c functions were thought to be of the form

$$b(N_{ss}) = \frac{k_1}{N_{ss}} + \frac{k_2}{\sqrt{N_{ss}}} + k_3 \qquad (7-6)$$

and

$$c(N_{ss}) = \frac{k_4}{N_{ss}} + \frac{k_5}{\sqrt{N_{ss}}} + k_6 \qquad (7-7)$$

where $k_1, k_2, \ldots, k_6$ are all constants. Matrix equations were then set up as follows:

$$\begin{bmatrix} b_1(N_{ss}) \\ b_2(N_{ss}) \\ \vdots \\ b_{16}(N_{ss}) \end{bmatrix} = \begin{bmatrix} \frac{1}{N_{ss_1}} & \frac{1}{\sqrt{N_{ss_1}}} & 1 \\ \frac{1}{N_{ss_2}} & \frac{1}{\sqrt{N_{ss_2}}} & 1 \\ \vdots & \vdots & \vdots \\ \frac{1}{N_{ss_{16}}} & \frac{1}{\sqrt{N_{ss_{16}}}} & 1 \end{bmatrix} \cdot \begin{bmatrix} k_1 \\ k_2 \\ k_3 \end{bmatrix} \qquad (7-8)$$

$$\begin{bmatrix} c_1(N_{ss}) \\ c_2(N_{ss}) \\ \vdots \\ c_{16}(N_{ss}) \end{bmatrix} = \begin{bmatrix} \frac{1}{N_{ss_1}} & \frac{1}{\sqrt{N_{ss_1}}} & 1 \\ \frac{1}{N_{ss_2}} & \frac{1}{\sqrt{N_{ss_2}}} & 1 \\ \vdots & \vdots & \vdots \\ \frac{1}{N_{ss_{16}}} & \frac{1}{\sqrt{N_{ss_{16}}}} & 1 \end{bmatrix} \cdot \begin{bmatrix} k_4 \\ k_5 \\ k_6 \end{bmatrix} \qquad (7-9)$$

The matrix computation software (CTRL–C [49]) computed the following constants in the functions:

$k_1 = 7.29082 \times 10^9$ $\qquad$ $k_4 = 1.39502 \times 10^9$

$k_2 = -1.86401 \times 10^5$ $\qquad$ $k_5 = 3.07719 \times 10^4$

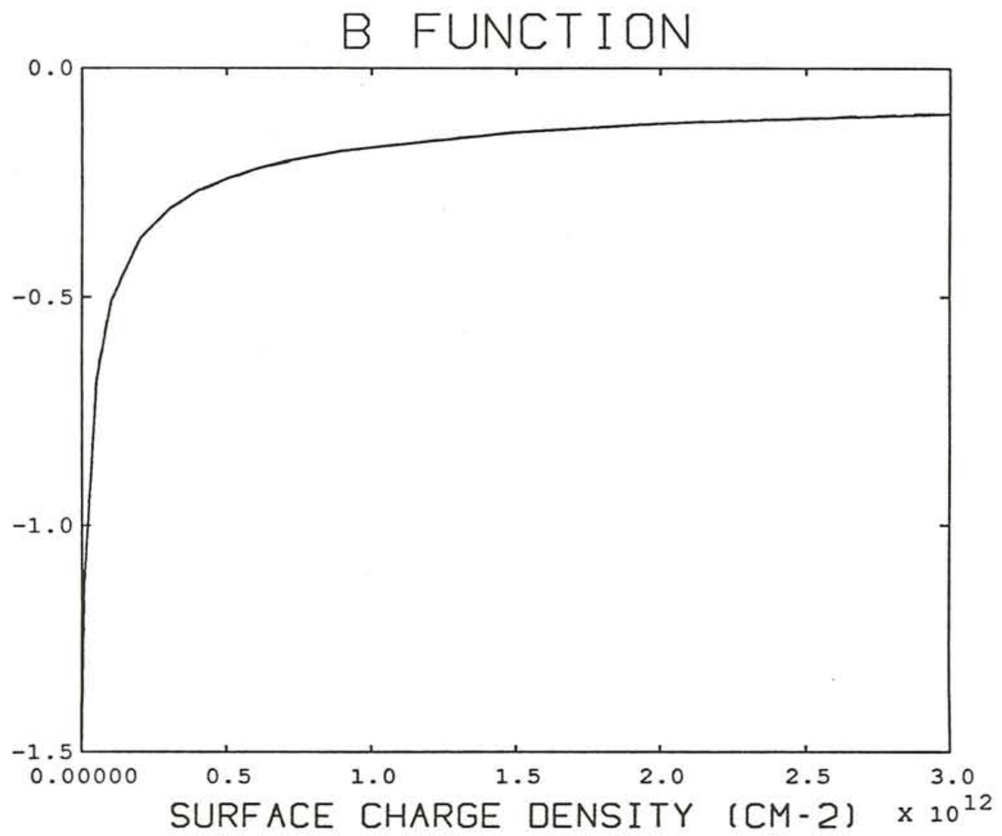


Figure 7-3. *b* function versus surface–charge density. Solid line represents experimental data and dashed line is reconstructed (curve–fitted) data.

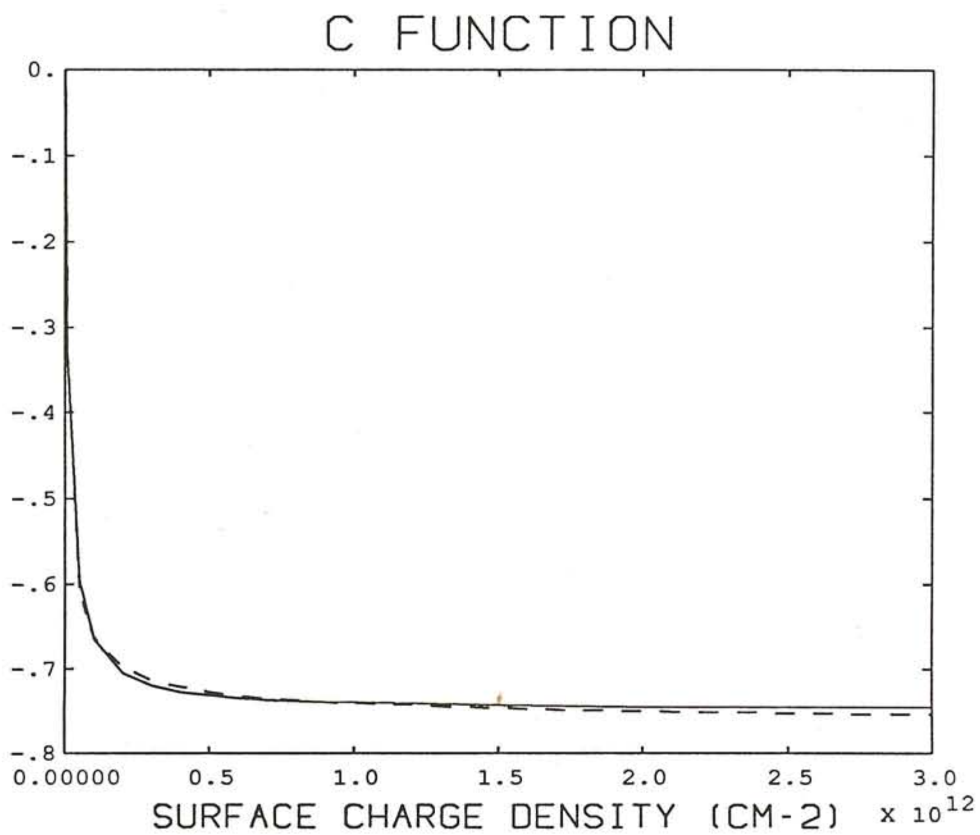


Figure 7-4. c function versus surface-charge density. Solid line represents experimental data and dashed line is reconstructed (curve-fitted) data.

$$k_3 = 9.60294 \times 10^{-3} \qquad k_6 = -0.773621$$

To check how accurate these expressions are, the $b(N_{ss})$ and $c(N_{ss})$ vectors were reconstructed using the functions just computed. The norm of the difference between the original and reconstructed b vectors is 0.005 and for the c vectors is 0.021. These are very small error–determining parameters which means that these computed functions describe the curves well. In Fig. (7-3), there is not a clear distinction between the experimental line (solid) and the curve–fitted line (dashed). The norm is a measure of "badness" and 0.005 is not bad at all. In Fig. (7-4), the curves are four times ($4 \times 0.005 = 0.02$) as bad which is evident in the way that there is a distinction between lines. It is not much error at all, though. Figs. (7-1) and (7-2) are reconstructed using these new functions and presented in Figs. (7-5) and (7-6) for comparisons.

These mathematical approximations were made so that they could be incorporated into the SEPSIP code to compute punch–through voltages between floating rings automatically. Before this feature can be added, the punch–through equation as a function of all three variables must be found. It is anticipated that this research shall be continued resulting in the punch–through equation being added to a future version of the code.

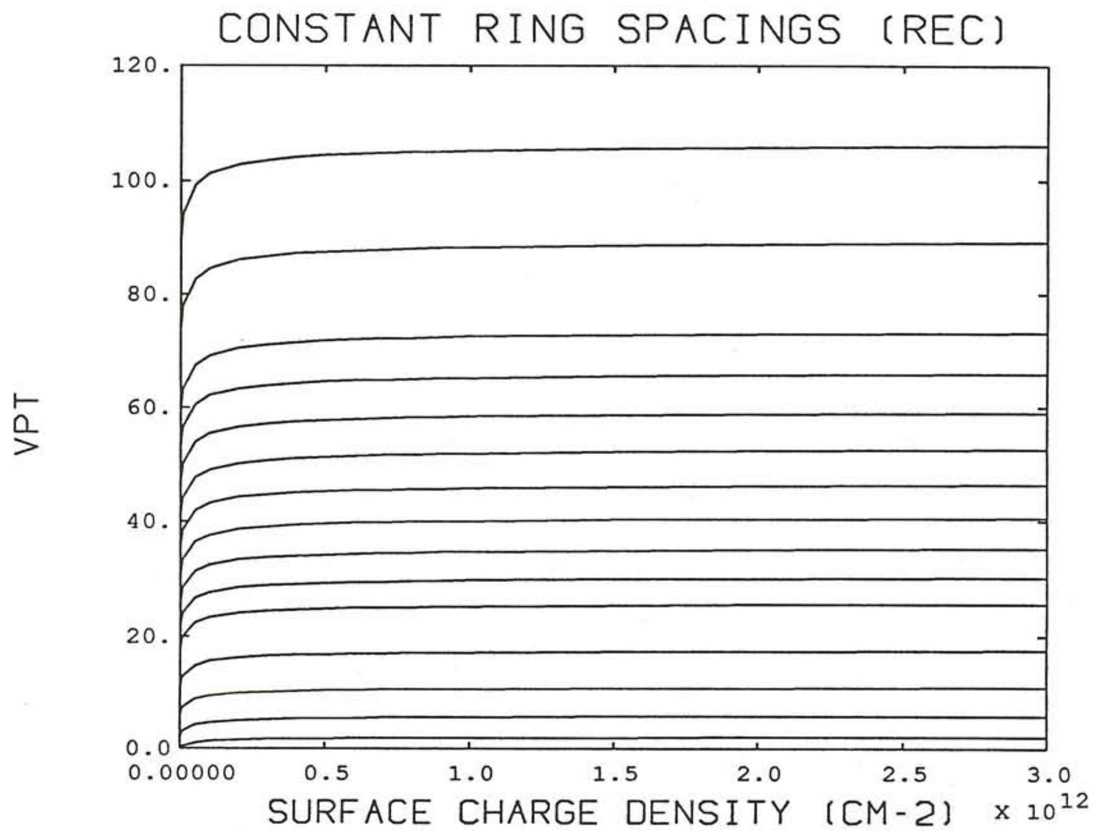


Figure 7-5. Punch–through voltage versus surface–charge density for constant ring spacings. This is reconstructed (from functions) data. Bottom curve is for 2-μm and the top curve is for 12-μm spacing.

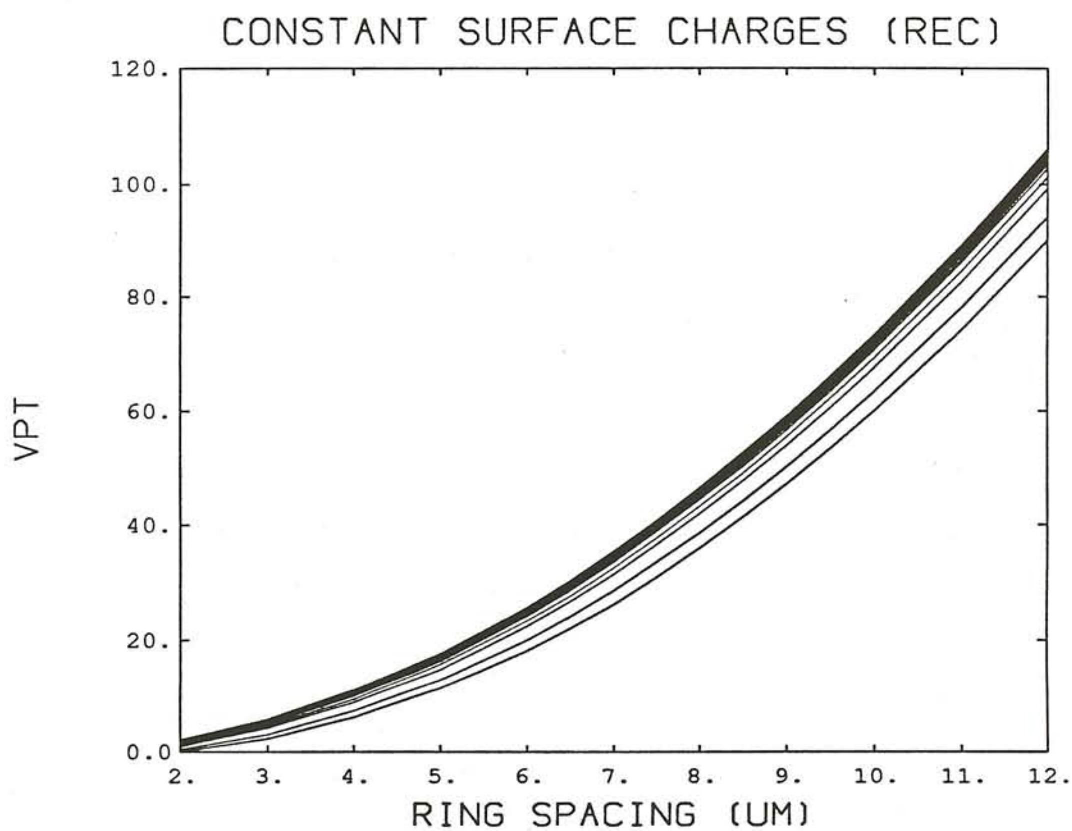


Figure 7-6. Punch–through voltage versus ring spacing for constant surface–charge densities. This is reconstructed (from functions) data. Bottom curve is for $0\,cm^{-2}$ and the top curve is for $3 \times 10^{12}\,cm^{-2}$ surface–charge density.

CHAPTER 8
CONCLUSIONS

The breakdown behavior of typical power–MOSFET termination structures was examined as a function of surface charge, and the results for selected structures were verified experimentally. The specific results presented are a function of doping profile and oxide thickness, but the approach is readily applicable to structures with other values of these parameters. A wide range of sensitivity to surface charge was found for different termination structures.

For a field plate to be effective in increasing the breakdown voltage, it is necessary to use an oxide thickness sufficiently large so that the depletion layer curvature is reduced and the peak electric field is moved lower in the semiconductor bulk. With a large oxide thickness, though, the structure is very sensitive to surface charge. The observed results are reasonable because field plates modify the potential distribution in the semiconductor by acting through an intervening dielectric layer. Any charge that is added in this dielectric layer produces a significant change in the potential in the semiconductor.

To achieve a high breakdown voltage and low sensitivity to surface charge, a device employing multiple field rings was found to work well. With just one ring, the breakdown voltage was substantially increased and sensitivity to surface charge was reduced. The optimal spacing of this ring was found to be 9.5 μm such that the breakdown voltage was maximized and the peak electric field minimized for the given impurity profile. The optimal spacing of a three–ring device was 7.5 μm between rings spaced uniformly. For avalanche multiplication to occur on all rings

simultaneously, the spacing of the rings should gradually increase as the distance from the main junction increases. This method of spacing the rings was used in the seven-ring device where the first ring was spaced $2.0\,\mu m$ from the main junction.

The trend is that as the number of rings in the device is increased, the spacing between these rings steadily decreases. This would suggest fabricating an optimal device with a large number of rings and very little spacing between them. The resulting structure would have a depletion layer approaching the optimal parallel-plane case, thus optimizing the breakdown voltage.

There is, however, obviously a tradeoff between die area, the desired increase in breakdown voltage, and the desired insensitivity to surface charge. The increase in breakdown voltage of an eight-ring device over a seven-ring device is very slight. The most appropriate number of rings will be determined by the application and by the radiation environment in which the device is to be deployed.

Great care must be taken when designing a power-MOSFET for use in an ionizing-radiation environment. SEPSIP has proven to be a valuable tool for this type of design work. It was found that multiple floating ring structures have the least sensitivity to radiation-induced charge of the structures examined. The spacing of these rings is critical because radiation-induced charge can render the outer rings ineffective if the distance between them is too large. By using SEPSIP with some initial insight as to what the spacing should be, one has a good starting point for determining the optimal ring spacing.

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